FORM 10-K/A

Annual report pursuant to section 13 and 15(d) [amend]

Filing Date: **2013-01-14** | Period of Report: **2012-06-30**
SEC Accession No. 0001103969-13-000006

FILER

MIPS TECHNOLOGIES INC
CIK:**1059786**| IRS No.: **770322161** | State of Incorp.:**DE** | Fiscal Year End: **0630**
Type: **10-K/A** | Act: **34** | File No.: **000-24487** | Film No.: **13526409**
SIC: **3674** Semiconductors & related devices

Mailing Address
955 EAST ARQUES AVENUE
SUNNYVALE CA 94085-4521

Business Address
955 EAST ARQUES AVENUE
SUNNYVALE CA 94085-4521
4085305000

UNITED STATES
SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549

FORM 10-K/A
(Amendment No. 2)

(Mark One)

☒ ANNUAL REPORT PURSUANT TO SECTION 13 OR 15 (d) OF THE SECURITIES EXCHANGE ACT OF 1934.

FOR THE FISCAL YEAR ENDED June 30, 2012

OR

☐ TRANSITION REPORT PURSUANT TO SECTION 13 OR 15 (d) OF THE SECURITIES EXCHANGE ACT OF 1934.

For the transition period from to .

Commission file number 000-24487

MIPS TECHNOLOGIES, INC.
(Exact name of registrant as specified in its charter)

DELAWARE	**77-0322161**
(State or other jurisdiction of Incorporation or organization)	(I.R.S. Employer Identification Number)

955 EAST ARQUES AVENUE, SUNNYVALE, CA 94085
(Address of principal executive offices)

Registrant's telephone number, including area code: **(408) 530-5000**

Securities registered pursuant to section 12(b) of the Act:

Title of Each Class	Name of Each Exchange on Which Registered
Common stock, $.001 Par Value Per Share	The Nasdaq Stock Market LLC

Securities registered pursuant to section 12(g) of the Act:

NONE

Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act. Yes ☐ No ☒

Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act. Yes ☐ No ☒

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes ☒ No ☐

Indicate by check mark whether the registrant has submitted electronically and posted on its corporate Web site, if any, every Interactive Data File required to be submitted and posted pursuant to Rule 405 of Regulation S-T (§232.405 of this chapter) during the preceding 12 months (or for such shorter period that the registrant was required to submit and post such files). ☒ Yes ♦ No

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K (§229.405 of this chapter) is not contained herein, and will not be contained, to the best of the Registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. ☒

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non-accelerated filer, or a smaller reporting Company. See the definition of "large accelerated filer," "accelerated filer" and "smaller reporting company" in Rule 12-b2 of the Exchange Act.

Large Accelerated filer ☐ Accelerated filer ☒ Non-accelerated filer ☐ Smaller reporting company ☐

Indicate by check mark whether the registrant is a shell company (as defined in Rule12b-2 of the Act). Yes ☐ No ☒

The aggregate market value of the voting and non-voting common equity held by non-affiliates computed by reference to the price at which the common equity was last sold as of the last business day of the registrant's most recently completed second fiscal quarter (December 31, 2011) was approximately $236 million for the registrant's common stock based on the closing sale price as reported on The Nasdaq Global Select Market.

As of December 31, 2012, the number of outstanding shares of the registrant's common stock, $0.001 par value, was 54,414,684.

DOCUMENTS INCORPORATED BY REFERENCE

None

EXPLANATORY NOTE

MIPS Technologies, Inc. is filing this Amendment No. 2 to our Annual Report on Form 10-K for the fiscal year ended June 30, 2012, filed with the Securities and Exchange Commission (SEC) on September 10, 2012 (Annual Report), which Annual Report was supplemented by Amendment No. 1 to the Annual Report, filed with the SEC on October 26, 2012, in response to comment letters received from the SEC in connection with its review of our application for confidential treatment for certain omitted portions of Exhibit 10.40.

Except as otherwise expressly stated in this Amendment No. 2, this Amendment No. 2 continues to speak as of the date of the Annual Report and we have not updated the disclosure contained herein to reflect events that have occurred since the filing of the Annual Report. Accordingly, this Amendment No. 2 should be read in conjunction with our Annual Report and any other filings we made with the SEC subsequent to the filing of the Annual Report.

PART IV

Item 15.*Exhibits and Financial Statement Schedules*

3. Exhibits. The following Exhibits are filed as part of, or incorporated by reference into, this Report:

Exhibit No.	List of Exhibits
3.1	Certificate of Incorporation (incorporated herein by reference to Exhibit 3.1 to the Company's Form 8-K filed on November 14, 2003).
3.2	Amended and Restated By-Laws (incorporated herein by reference to Exhibit 3.1 to the Company's Form 8-K filed on August 18, 2010).
4.1	Amended and Restated Preferred Stock Rights Agreement, as amended (incorporated herein by reference to Exhibit 10.11.3 to the Company's Form 8-A12G/A filed on November 18, 2003).
10.1	The Amended and Restated Separation Agreement between the Company and Silicon Graphics, Inc. (incorporated herein by reference to Exhibit 10.1 to the Company's Annual Report on Form 10-K for the year ended June 30, 1999).
10.2	The Corporate Agreement between the Company and Silicon Graphics, Inc. (incorporated herein by reference to Exhibit 10.2 to the Registration Statement on Form S-1, Registration No. 333-73071 (the "Registration Statement")).
10.3	The Management Services Agreement between the Company and Silicon Graphics, Inc. (incorporated herein by reference to Exhibit 10.3 to the Registration Statement).
10.4	The Tax Sharing Agreement between the Company and Silicon Graphics, Inc. (incorporated herein by reference to Exhibit 10.4 to the Registration Statement).
10.5	The Technology Agreement between the Company and Silicon Graphics, Inc. (incorporated herein by reference to Exhibit 10.5 to the Registration Statement).
10.6	The Trademark Agreement between the Company and Silicon Graphics, Inc. (incorporated herein by reference to Exhibit 10.6 to the Registration Statement).
10.7	The Tax indemnification Agreement between the Company and Silicon Graphics, Inc. (incorporated herein by reference to Exhibit 10.11 to the Company's Annual Report on Form 10-K for the year ended June 30, 2000).
10.8*	The 1998 Long-Term Incentive Plan, as amended and restated (incorporated herein by reference to Exhibit 99.01 to the Company's Form S-8 filed on May 10, 2012).
10.9*	The Employee Stock Purchase Plan, as amended (incorporated herein by reference to Exhibit 4.03 to the Company's Current Report on Form 8-K filed on January 11, 2008).
10.10*	Directors' Stock Option Plan, as amended (incorporated herein by reference to Exhibit 10.10 to the Company's Quarterly Report on Form 10-Q for the quarter ended March 31, 2002).
10.11*	Nonqualified Deferred Compensation Plan (incorporated herein by reference to Exhibit 10.12 to the Company's Quarterly Report on Form 10-Q for the quarter ended December 31, 2000).
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10.14*	Form of Award Document, as amended for Stock Option Grant to Employee under the 1998 Long-Term Incentive Plan comprised of Stock Option Agreement and Exercise Notice (incorporated herein by reference to Exhibit 10.14 to the Company's Annual Report on Form 10-K for the year ended June 30, 2010).
10.15*	Form of Award Document for Restricted Stock Purchase Agreement under the 1998 Long-Term Incentive Plan (incorporated herein by reference to Exhibit 10.18 to the Company's Annual Report on Form 10-K for the year ended June 30, 2004).
10.16*	Form of Award Document for Director Stock Option Agreement (Initial Grant) under the Directors' Stock Option Plan (incorporated herein by reference to Exhibit 10.19 to the Company's Annual Report on Form 10-K for the year ended June 30, 2004).
10.17*	Form of Award Document for Director Stock Option Agreement (Renewal Grant) under the Directors' Stock Option Plan (incorporated herein by reference to Exhibit 10.20 to the Company's Annual Report on Form 10-K for the year ended June 30, 2004).
10.18*	Form of Award Document, as amended for Stock Option Grant to International Employee under the 1998 Long-Term Incentive Plan comprised of Stock Option Agreement and Exercise Notice (incorporated herein by reference to Exhibit 10.18 to the Company's Annual Report on Form 10-K for the year ended June 30, 2010).
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10.20*	Form of Stock Unit Award Agreement for Members of the Board of Directors (incorporated herein by reference to Exhibit 10.1 to the Company's Form 8-K filed on February 12, 2010).
10.21*	Form of Stock Unit Award Agreement for Employees Outside the U.S. (incorporated herein by reference to Exhibit 10.2 to the Company's Quarterly Report on Form 10-Q for the quarter ended December 31, 2010).
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10.25*	Change in Control Agreement (incorporated herein by reference to Exhibit 99.03 to the Company's Current Report on Form 8-K filed on October 16, 2007).
10.26*	Amendment to Change in Control Agreement (incorporated herein by reference to Exhibit 10.2 to the Company's Quarterly Report on Form 10-Q filed on February 6, 2009).

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10.28*	Offer Letter dated December 22, 2009 to Sandeep Vij (incorporated herein by reference to Exhibit 99.02 to the Company's Form 8-K filed on January 25, 2010).
10.29*	Offer Letter dated March 10, 2010 to Ravikrishna Cherukuri, Vice President of Engineering (incorporated herein by reference to Exhibit 10.3 to the Company's Form 10-Q filed on May 6, 2010).
10.30*	Letter Agreement and Transition Agreement between MIPS Technologies, Inc. and Sandy Creighton (incorporated herein by reference to Exhibit 10.2 to the Company's Quarterly Report on Form 10-Q for the quarter ended September 30, 2010).
10.31*	Consulting Agreement between MIPS Technologies, Inc. and Sandy Creighton (incorporated herein by reference to Exhibit 10.3 to the Company's Quarterly Report on Form 10-Q for the quarter ended September 30, 2010).
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10.36*	Consulting Agreement between MIPS Technologies, Inc. and Arthur Swift (incorporated herein by reference to Exhibit 10.5 to the Company's Quarterly Report on Form 10-Q for the quarter ended September 30, 2011).
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23.1	Consent of Independent Registered Public Accounting Firm (incorporated herein by reference to exhibit 23.1 to the Company's Annual Report on Form 10-K for the year ended June 30, 2012).
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31.5	Certification of Chief Executive Officer pursuant to Section 302 of the Sarbanes-Oxley Act of 2002.
31.6	Certification of Chief Financial Officer pursuant to Section 302 of the Sarbanes-Oxley Act of 2002.
32.1	Certification of Chief Executive Officer pursuant to Section 906 of the Sarbanes-Oxley Act of 2002 (incorporated herein by reference to exhibit 32.1 to the Company's Annual Report on Form 10-K for the year ended June 30, 2012)
32.2	Certification of Chief Financial Officer pursuant to Section 906 of the Sarbanes-Oxley Act of 2002 (incorporated herein by reference to exhibit 32.2 to the Company's Annual Report on Form 10-K for the year ended June 30, 2012)

* Management contract or compensatory plan or arrangement required to be filed as an exhibit to this Annual Report on Form 10-K pursuant to Item 15(b) of said form.

** Portions of this exhibit have been omitted in conjunction with a confidential treatment application filed with the Securities and Exchange Commission.

SIGNATURES

Pursuant to the requirements of Section 13 or 15 (d) of the Securities Exchange Act of 1934, the registrant has duly caused this Report to be signed on its behalf by the undersigned, thereunto duly authorized.

MIPS Technologies, Inc.

By: /s/ SANDEEP VIJ
Sandeep Vij
President and Chief Executive Officer.

Date: January 11, 2013

Pursuant to the requirements of the Securities Exchange Act of 1934, this Report has been signed below by the following persons on behalf of the Registrant and in the capacities and on the dates indicated.

Signature	Title	Date
/s/ SANDEEP VIJ Sandeep Vij	Chief Executive Officer and Director (Principal Executive Officer)	January 11, 2013
/s/ WILLIAM SLATER William Slater	Vice President and Chief Financial Officer (Principal Financial and Accounting Officer)	January 11, 2013
/s/ KENNETH L. COLEMAN Kenneth L. Coleman	Director and Chairman of the Board	January 11, 2013
/s/ FRED M. GIBBONS Fred M. Gibbons	Director	January 11, 2013
/s/ ROBERT R. HERB Robert R. Herb	Director	January 11, 2013
/s/ WILLIAM M. KELLY William M. Kelly	Director	January 11, 2013
/s/ JEFFREY MCCREARY Jeffrey McCreary	Director	January 11, 2013
/s/ KENNETH TRAUB Kenneth Traub	Director	January 11, 2013
/s/ ROBIN L. WASHINGTON Robin L. Washington	Director	January 11, 2013
/s/ FRED WEBER Fred Weber	Director	January 11, 2013

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* Management contract or compensatory plan or arrangement required to be filed as an exhibit to this Annual Report on Form 10-K pursuant to Item 15(b) of said form.

** Portions of this exhibit have been omitted in conjunction with a confidential treatment application filed with the Securities and Exchange Commission.

EXHIBIT 10.40

CONFIDENTIAL TREATMENT REQUESTED. CERTAIN PORTIONS OF THIS DOCUMENT HAVE BEEN OMITTED PURSUANT TO A REQUEST FOR CONFIDENTIAL TREATMENT AND, WHERE APPLICABLE, HAVE BEEN MARKED WITH AN ASTERISK TO DENOTE WHERE OMISSIONS HAVE BEEN MADE. THE CONFIDENTIAL MATERIAL HAS BEEN FILED SEPARATELY WITH THE SECURITIES AND EXCHANGE COMMISSION.

LICENSE AGREEMENT

This LICENSE AGREEMENT (this "Agreement") is made and entered into as of June 29, 2012 (the "Effective Date") by and between MIPS Technologies, Inc., a Delaware corporation having its principal office at 955 East Arques Avenue, Sunnyvale, California 94085 ("MIPS"), and Broadcom Corporation, a corporation organized and existing under the laws of California, having its principal office at 5300 California Ave., Irvine, California 92617 ("Broadcom") (MIPS and Broadcom are individually referred to herein as a "party," and collectively as the "parties").

WITNESSETH

WHEREAS, MIPS and Broadcom have previously entered into certain license agreements under which Broadcom has obtained licenses to the MIPS microprocessor architectures and cores ("MIPS Technology Licenses");

WHEREAS, MIPS and Broadcom are concurrently entering into amendments to the MIPS Technology Licenses as attached hereto as Attachments 1, 2 and 3 to, among other things, extend the term of such licenses; and

WHEREAS, MIPS wishes to grant to Broadcom, and Broadcom wishes to acquire, a worldwide, non-exclusive license under certain patents on the terms and conditions described herein.

NOW, THEREFORE, in consideration of the above and the mutual covenants and promises hereinafter contained, the parties agree as follows:

ARTICLE I – DEFINITIONS

As used in this Agreement, the following terms shall have the following meanings:

1.1 "Affiliate" means, with respect to a party, any other Person that directly, or indirectly through one or more intermediaries, is Controlled by such specified party at any time during the term of this Agreement, but only so long as such Control exists, and subject to Section 6.3 below.

1.2 "Assert" (or "Assertion") means to initiate or pursue an action before any legal, judicial, arbitration, administrative, executive or other type of body or tribunal, anywhere in the world, that has or claims to have authority to adjudicate such action.

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

1.3 "Broadcom Licensed Product" means any past, present or future product or service, including hardware, software, firmware, cores, and reference designs, (a) in which Broadcom or its Affiliates [*] with respect to the [*], but which may [*] by [*]; or (b) that is a [*]; or (c) that is [*] or [*] of Broadcom or its Affiliates based on [*] Broadcom or its Affiliates; or (d) that is based [*] Broadcom or its Affiliates and [*] under a [*] by Broadcom or its Affiliates, including, without limitation, the [*] by Broadcom [*] its products.

1.4 "Broadcom Customers" means any Third Parties that purchase or otherwise lawfully obtain any Broadcom Licensed Products, and that are one of Broadcom's or its Affiliates' direct or indirect customers, retailers, wholesalers, distributors, dealers, resellers, users, original equipment manufacturers, importers, exporters, or original design manufacturers, including telecommunications carriers, network operators and end users who may lawfully obtain Broadcom Licensed Products from any of the foregoing.

1.5 "Broadcom Suppliers" means any Third Party that provides products or services to Broadcom or its Affiliates, which product or service, as applicable, forms a part of, or is incorporated into, or is used for the manufacture or test of any Broadcom Licensed Products, including Broadcom's and its Affiliates' direct and indirect suppliers, manufacturers, contractors, assembly facilities, and testing facilities.

1.6 "Capture Period" means any time on or prior to the [*].

1.7 "Claims" means claims, counterclaims and cross-claims, as well as any and all actions, causes of action, costs, damages, debts, demands, expenses, liabilities, losses, obligations, proceedings, and suits of every kind and nature, liquidated or unliquidated, fixed or contingent, in law, equity or otherwise and whether presently known or unknown.

1.8 "Control" means: (i) the direct or indirect ownership of more than fifty percent (50%) of the outstanding shares or securities entitled to vote for the election of directors or similar managing authority of a Person; or (ii) the direct or indirect ownership of more than fifty percent (50%) of the aggregate Voting Power of a Person; or (iii) other right, authority or power to direct the management, operation, or policies of such Person.

1.9 "Custom ICs" means integrated circuit products (ICs) [*] Third Party [*] (whether or not branded or co-branded with such Third Party) where: (i) Broadcom or its Affiliate conducted [*] with respect to such ICs or the [*] used in such ICs; and (ii) the [*] conducted by Broadcom or its Affiliate includes [*].

1.10 "Licensed Patents" means all Patents that are: (i) owned, [*], by MIPS or by any of its Affiliates [*] (including any Patents [*] Third Parties); or (ii) licensable, [*], by MIPS or by any of its Affiliates [*] of or within the scope granted herein without requiring [*] to [*] (except [*] to [*] for inventions made by [*] while [*]); or (iii) any Patent that claims priority directly or indirectly from, or from which priority is directly or indirectly claimed by, any of the foregoing Patents under (i) or (ii) above, and all continuations, divisionals, continuations-in-part, foreign counterparts, reexaminations, reissues, substitutes, extensions and renewals of any of the foregoing. The Licensed Patents include, but are not limited to, the Patents listed in Exhibit A

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and all Patents related as described under (iii) above to the Patents listed in Exhibit A (collectively, the "Listed Patents").

1.11 "Patents" means (i) all classes or types of patents, including utility patents, utility models, design patents, invention certificates, continuations, divisionals, continuations-in-part, foreign counterparts, reexaminations, reissues, substitutes, extensions and renewals, in all countries of the world; and (ii) all applications, and rights to inventions for which applications may be filed, for these classes or types of patents in all countries of the world.

1.12 "Person" means an individual, trust, corporation, partnership, limited liability company, association, unincorporated organization or other legal or governmental entity.

1.13 "Sell" (including "Sold" and other forms) means to sell, lease, distribute or otherwise transfer or dispose of a product or item (directly and indirectly through multiple tiers of distribution) or to provide or deliver a service.

1.14 "Third Party" means a Person other than a party to this Agreement.

1.15 "Voting Power" means the direct or indirect right to exercise voting power (including by written proxy) with respect to the election of directors or similar managing authority of a Person (whether through direct or indirect beneficial ownership of shares or securities of such Person, the right to direct the vote in such elections (including by written proxy), or otherwise).

ARTICLE II – RELEASES

2.1 MIPS Release.

(a) MIPS, on behalf of itself and its Affiliates, irrevocably releases, acquits and forever discharges Broadcom and its Affiliates and each of their respective officers, directors, employees, agents, successors, assigns, representatives, and attorneys (collectively, the "Broadcom Releasees") from and against any and all Claims which MIPS or its Affiliates may have or obtain that any act undertaken by or for any of the Broadcom Releasees prior to the Effective Date infringes any Patent (whether direct, contributory or by inducement, and whether or not willful), including any infringement, or alleged infringement of any Licensed Patents (whether direct, contributory or by inducement, and whether or not willful), and including as relating to or based on any Broadcom Licensed Products (or the manufacture, use, Sale, offer for Sale, import, export or other exploitation thereof). For the avoidance of doubt, nothing in this Section 2.1 is intended to or shall release Broadcom or any of its Affiliates from any obligations under this Agreement.

(b) Third Parties. MIPS, on behalf of itself and its Affiliates, irrevocably releases, acquits and forever discharges the Broadcom Customers and Broadcom Suppliers from and against any and all Claims which MIPS or its Affiliates may have or obtain for infringement of the Licensed Patents (whether direct, contributory or by inducement, and whether or not willful) to the extent such infringement arises from (i) the use, sale, offer for sale, or import by or for any Broadcom Customer of any Broadcom Licensed Product Sold by or for Broadcom or any of its

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Affiliates, but solely to the extent such infringing activity would have been covered by the licenses or covenants granted in Section 3 if such activity occurred after the Effective Date, or (ii) the manufacture or supply by any Broadcom Supplier of any Broadcom Licensed Product (or any component thereof) to or on behalf of Broadcom or any of its Affiliates, but solely to the extent such infringing activity would have been covered by the licenses or covenants granted in Section 3 if such activity occurred after the Effective Date.

2.2 Broadcom Release.

(a) Broadcom, on behalf of itself and its Affiliates, irrevocably releases, acquits and forever discharges MIPS and its Affiliates and their respective officers, directors, employees, agents, successors, assigns, representatives, and attorneys from any and all Claims for indemnification by Broadcom and its Affiliates arising in connection with U.S. Patent [*] asserted by [*], including in connection with the matter styled [*] pending in the United States District Court for the District of [*]).

(b) The Parties acknowledge and agree that as of the Effective Date, and subject to the release set forth in Section 2.2(a) above, MIPS' liabilities and Broadcom's remedies for patent infringement indemnification under the MIPS Technology Licenses shall be subject to the limitations set forth in the amendments to such MIPS Technology Licenses attached hereto. Neither Broadcom nor its Affiliates may bring any patent infringement indemnification claim against MIPS or its Affiliates under such MIPS Technology Licenses except as expressly permitted under such MIPS Technology Licenses, as so amended.

2.3 Waiver. Each Party and its Affiliates expressly, knowingly and intentionally waive for themselves and their legal successors and assigns, the benefits and rights of Section 1542 of the California Civil Code, which states as follows:

> ***"A GENERAL RELEASE DOES NOT EXTEND TO CLAIMS WHICH THE CREDITOR DOES NOT KNOW OR SUSPECT TO EXIST IN HIS OR HER FAVOR AT THE TIME OF EXECUTING THE RELEASE, WHICH IF KNOWN BY HIM OR HER MUST HAVE MATERIALLY AFFECTED HIS OR HER SETTLEMENT WITH THE DEBTOR."***

Each Party and its Affiliates acknowledge that they have received independent legal advice from their attorneys with respect to waiving the provisions of California Civil Code § 1542 and acknowledge that this waiver is a material inducement to and consideration for the other party's execution of the Agreement. Each Party and its Affiliates likewise waive the benefits of any statute, rule, doctrine or common law principle of any jurisdiction of similar effect to Section 1542 of the California Civil Code.

ARTICLE III – LICENSES AND COVENANTS

3.1 License Grants.

(a) Licensed Patents. MIPS (on behalf of itself and its Affiliates) hereby grants to Broadcom and each of its Affiliates a fully paid-up and royalty-free, non-assignable (except as

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provided in ARTICLE VI), non-transferable (except as provided in ARTICLE VI), irrevocable, non-terminable (except as set forth in Section 5.1 below), non-exclusive, worldwide license, without the right to sublicense, under the Licensed Patents, to (i) make, have made, use, Sell, offer to Sell and import Broadcom Licensed Products, (ii) practice any process, method, or procedure claimed in the Licensed Patents in connection with such manufacture, use, Sale, offer to Sell or import of the Broadcom Licensed Products, and (iii) make, have made, use, import and otherwise practice under the Licensed Patents for Broadcom's or any of its Affiliates' internal use or internal business operations.

(b) Contractors; Third Party Service Providers. The license set forth in this Section 3.1 includes the right for Broadcom and its Affiliates to have the license rights exercised on its behalf by contractors and Third Party service providers solely in connection with the provision of services to Broadcom or its Affiliates.

(c) Software. The license set forth in this Section 3.1 shall be deemed to extend to and cover software provided by Broadcom and its Affiliates [*] Broadcom Licensed Products, including the right for Broadcom and its Affiliates to directly and indirectly grant Third Parties (and authorize such Third Parties to grant) rights to use, reproduce, modify, prepare derivative works of, distribute (directly and indirectly through multiple tiers of distribution) and otherwise exploit such software [*] in connection with Broadcom Licensed Products and [*] contained in the software [*] Broadcom or its Affiliates or otherwise relating to the [*] the Broadcom Licensed Product.

(d) Combinations. The license set forth in this Section 3.1 shall be deemed to extend to and cover any combination or use of a [*] by [*] together with a product, service or other item that is not a [*] (a "Combination") [*].

(e) No Foundry Rights. The parties acknowledge and agree that the covenants and licenses in this Agreement are intended to cover only Broadcom Licensed Products and are not intended to cover any foundry manufacturing activities which Broadcom or any of its Affiliates may undertake for or on behalf of any Third Party based on IC designs provided by such Third Party in substantially completed form.

3.2 Exhaustion. MIPS expressly recognizes, agrees and acknowledges that the licenses and covenants granted by this Agreement shall fully exhaust (based on principles of, and solely to the extent of, patent exhaustion under U.S. law) MIPS' rights under all claims of the Licensed Patents relating to the Broadcom Licensed Products not only as to Broadcom and its Affiliates, but also as to all Broadcom Customers and Broadcom Suppliers. Such exhaustion shall apply on a worldwide basis regardless of where the Broadcom Licensed Product is made, used or first sold (e.g., regardless of whether first sold in the United States or a foreign country). This Agreement in no way limits or restricts the Broadcom Customers to which Broadcom or its Affiliates are entitled to sell Broadcom Licensed Products.

3.3 Covenants Not to Sue.

(a) MIPS and its Affiliates covenant not to Assert any Claim against (i) Broadcom or any of its Affiliates, for infringement of any Licensed Patent (whether direct, contributory or by

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inducement, and whether or not willful) resulting from the use, manufacture, Sale, offer to Sell or import of any Broadcom Licensed Product, regardless of whether such Claim arose before or after the Effective Date, but only to the extent such use, manufacture, Sale or import of the applicable Broadcom Licensed Product, would, if it occurred after the Effective Date, be within the scope of the license set forth in Section 3.1.

(b) MIPS and its Affiliates covenant not to Assert any Claim against (i) any Broadcom Supplier for infringement of any Licensed Patent (whether direct, contributory, by inducement, and whether or not willful) resulting from the manufacture or supply of any Broadcom Licensed Product to or on behalf of Broadcom or any of its Affiliates, regardless of whether such Claim arose before or after the Effective Date, but only to the extent such manufacture or supply of the applicable Broadcom Licensed Product, would, if it occurred after the Effective Date, be within the scope of the license set forth in Section 3.1 and (ii) any Broadcom Customer for infringement of any Licensed Patent (whether direct, contributory, by inducement, and whether or not willful) resulting from the use, Sale, offer to Sell or import of any Broadcom Licensed Product Sold by or for Broadcom or any of its Affiliates, regardless of whether such Claim arose before or after the Effective Date, but only to the extent such use, Sale, offer to Sell or import of the applicable Broadcom Licensed Product, would, if it occurred after the Effective Date, be within the scope of the license set forth in Section 3.1. The covenant not to sue in this Section 3.3(b) shall apply only with respect to Broadcom Licensed Products and shall not apply to i) any products or services of any Third Party or ii) any Combination that is outside the scope of Section 3.1(d). If a [*] MIPS or any of its Affiliates for a Patent [*] by such [*] (prior to [*] by MIPS or its Affiliates [*]), then the [*] of [*] under this Section 3.3(b) will be [*] while such Assertion remains pending; provided, however, that the foregoing will not be construed as [*] limiting the releases in Section 2.1, the license granted in Section 3.1 or the covenant granted in Section 3.3(a) above. In the event of a breach of the covenant set forth in this Section 3.3(b), MIPS or its respective Affiliate will have [*] by dismissing the respective Claim that was Asserted in violation of this Section 3.3(b).

3.4 No Other Rights. No releases, rights or licenses are granted under any Licensed Patents except as expressly provided in Section 2.1 and this Section 3, whether by implication, estoppel or otherwise, and except as expressly provided in Section 2.1 and this Section 3, nothing contained in this Agreement is intended to confer by implication, estoppel, or otherwise, upon Broadcom, any of its Affiliates, or any other Person, a license or rights in any intellectual property rights of MIPS or any of its Affiliates. Notwithstanding anything to the contrary, nothing in this Agreement shall be construed as granting or conveying any release, license, covenant or other right under or with respect to any Patents of Broadcom or any of its Affiliates, whether expressly, by implication, estoppel or otherwise.

3.5 Other Patents. If, [*], MIPS or any of its Affiliates [*] or [*] of any [*] directly or indirectly to any date within the Capture Period that is not [*], then MIPS and/or such Affiliate shall not take any action at any time during the term to enforce or consent to or permit the enforcement of such Patent against Broadcom or its Affiliates or with respect to any Broadcom Licensed Product to the extent the allegedly infringing activity is within the scope that would have been subject to the license set forth in Section 3.1 if the Patent had [*]. If a Patent that would otherwise qualify as [*] but does not solely as a result of the fact that such Patent is [*] (other than [*]), Broadcom shall have the right to include such Patent under the releases and

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licenses granted to Broadcom and its Affiliates under this Agreement [*] agrees to [*] required to [*] by reason of such [*].

3.6 Affiliates. Each party shall ensure that all of its Affiliates are bound by the applicable releases, covenants, and licenses under this Agreement.

3.7 Further Assurances. Each party hereby agrees to execute any further documents, including any declaration, oath, affidavit, assignment, confirmation or other instrument reasonably necessary or appropriate to complete, effectuate or give full effect to the release, license rights and/or covenants not to sue granted to the other party in this Agreement.

ARTICLE IV – CONSIDERATION

4.1 Payment Amount. In consideration of the releases, licenses and covenants granted by MIPS hereunder, Broadcom shall pay to MIPS a total amount of Twenty Six Million, Five Hundred Thousand United States Dollars ($26,500,000), on the terms and schedule set forth in Section 4.2 below. The foregoing payment (totaling $26,500,000) shall be the sole remuneration to MIPS under this Agreement and Broadcom and its Affiliates shall not be required to make any other payments under this Agreement or in connection with the Licensed Patents.

4.2 Payment Date. The payment amount identified in Section 4.1 above is due and payable on the Effective Date, and shall be paid within five (5) business days after the Effective Date. On or before five (5) business days after the Effective Date, Broadcom shall pay, or shall cause its designee to pay, MIPS the amount identified in Section 4.1 above by wire transfer to: [*]. Broadcom shall have sole discretion over allocation of the payment obligation between Broadcom and any of its Affiliates.

ARTICLE V – TERM AND REMEDIES FOR BREACH

5.1 Term. The term of this Agreement shall commence upon the Effective Date and shall continue until the expiration of the last to expire of the Licensed Patents, unless earlier terminated for uncured breach of Broadcom's payment obligation as expressly set forth below. In no event shall rescission or termination of this Agreement be a remedy for any breach hereof by either party, except that MIPS shall have the right to terminate this Agreement upon notice to Broadcom, if Broadcom fails to pay the amount set forth in Section 4.1 and fails to cure such non-payment within [*] after receipt of notice thereof. Upon payment of the amount set forth in Section 4.1, the rights and licenses granted to Broadcom and its Affiliates under this Agreement shall be irrevocable and non-terminable by MIPS or any of its Affiliates for any reason.

5.2 Defense to Infringement Claims. This Agreement may be offered in evidence and pleaded as an affirmative defense to any Claims that may be instituted, prosecuted, or attempted that Broadcom, any of its Affiliates, or any Broadcom Licensed Product infringes any Licensed Patent. In any such action, and in any action to enforce this Agreement, the prevailing person or entity shall recover its reasonable attorneys' fees and costs. Any filing of this Agreement in such a proceeding shall be done under seal.

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5.3 Remedies. The parties acknowledge and agree that, subject to Section 5.1: (i) any breach of this Agreement may result in immediate and irreparable injury for which there may be no adequate remedy available at law; and (ii) in addition to any other remedies available, specific performance and injunctive relief may be appropriate remedies to compel performance of this Agreement.

ARTICLE VI – ASSIGNMENT AND TRANSFER

6.1 Transfer of Licensed Patents. MIPS agrees, on behalf of itself and its Affiliates, that all of the licenses, releases, covenants not to sue and other rights granted by them and all their obligations set forth in this Agreement that relate to the Licensed Patents (the "Patent Obligations") shall run with any Licensed Patents that are transferred. MIPS shall ensure that any assignee, transferee or successor to any of the Licensed Patents (including the acquiring or surviving entity in connection with any acquisition or other Change of Control of MIPS), or any other entity (such as an exclusive licensee) that obtains any enforcement rights with respect to any of the Licensed Patents is notified in advance of and agrees in writing, prior to or as part of such assignment, transfer or grant, to be bound by all such Patent Obligations (including the obligation to obtain such written agreement from any subsequent assignee, transferee, successor or grantee).

6.2 Former MIPS Affiliates. If an Affiliate of MIPS that holds any Licensed Patent ceases to be an Affiliate of MIPS (a "Former MIPS Affiliate"), such rights and licenses granted by such Former MIPS Affiliate (including every successor entity in interest to any such patents or utility models and applications therefor) during the time such entity was a MIPS Affiliate shall continue in accordance with the terms of this Agreement after such entity becomes a Former MIPS Affiliate.

6.3 Former Broadcom Affiliates. If an Affiliate of Broadcom ceases to be an Affiliate of Broadcom (a "Former Broadcom Affiliate"), the rights and licenses granted to such Former Broadcom Affiliate will remain in effect, but will be limited to and shall apply solely with respect to those Broadcom Licensed Products that have been made commercially available prior to or at the time it becomes a Former Broadcom Affiliate and error corrections and minor enhancements thereto ("Existing Products"). Notwithstanding anything to the contrary, the parties acknowledge and agree that no right, license, or interest in or to any Licensed Patent does or shall extend to the acquirer, successor, assign, or other Third Party (each a "Successor Entity") by reason of participating in any acquisition or similar transaction in which the Former Broadcom Affiliate ceases to be an Affiliate of Broadcom ("Divestiture Transaction"), including any rights as to any past, present or future product or service of the Successor Entity except for the rights and license granted to the applicable Former Broadcom Affiliate in connection with the Existing Products of such Former Broadcom Affiliate. Nothing in this Section 6.3 shall be construed as limiting any of the rights and licenses granted to Broadcom, or to any of its Affiliates who remain Affiliates of Broadcom after the respective Divestiture Transaction, which shall remain in effect without restriction.

6.4 New Broadcom Affiliates. If a Third Party that recognizes and reports annual revenue, as measured in accordance with United States generally accepted accounting principles ("GAAP") or International Financial Reporting Standards ("IFRS"), that are [*] becomes an Affiliate of Broadcom [*], the licenses, covenants and releases under this Agreement will automatically extend to such Third Party at the time [*]. If a Third Party that recognizes and reports annual revenue, as measured in accordance with GAAP or IFRS, that are [*] becomes an

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Affiliate of Broadcom [*], the licenses and covenants under this Agreement will automatically extend to such Person at the time [*] with respect to products and services meeting the definition of [*] on or after such time; provided, however, that (i) if MIPS or its Affiliate has Asserted a Claim of infringement of a Licensed Patent against such Third Party in patent litigation pending as of the date of the transaction or series of related transactions under which the Third Party will become an Affiliate of Broadcom ("Acquisition"), then the products of such Third Party accused of infringing the Licensed Patents in such action ("Accused Products") will not be considered to become [*] under this Agreement by reason of such Acquisition and this Agreement will not be construed as preventing MIPS or its Affiliate from continuing to pursue such litigation against the Third Party with respect to the Accused Products; and (ii) the releases under this Agreement will not be extended to such Person for activities prior to the time that such Person becomes [*]. As used above, [*] means [*] then-current annual revenues, in each case as measured over the preceding [*] at the time the respective Person becomes an Affiliate.

6.5 Assignment. This Agreement and the rights and licenses granted herein shall inure to the benefit of the parties and their permitted successors and assigns. Neither party to this Agreement shall assign or transfer any of its rights or privileges hereunder without the prior written consent of the other party, except that either party may assign this Agreement without the other party's consent to a successor to all or substantially all of its business or assets to which this Agreement relates, whether by merger, acquisition or other transaction or series of related transactions. In the event of a Change of Control of Broadcom, the parties acknowledge and agree to the following: the rights and licenses granted to Broadcom under this Agreement with respect to Broadcom Licensed Products will remain in effect prospectively solely with respect to past, present and future Broadcom Licensed Products of (i) Broadcom or its surviving successor entity itself in such Change of Control transaction ("Surviving Broadcom Entity") and (ii) the Affiliates of Broadcom prior to such Change of Control who are or become Affiliates of the Surviving Entity as a result of such Change of Control transaction ("Surviving Broadcom Affiliates"), but will not extend to any past, present or future product or service of the Third Party involved in the Change of Control transaction (other than the Surviving Broadcom Entity and Surviving Broadcom Affiliates) ("Acquirer"). Notwithstanding anything to the contrary, the parties acknowledge and agree that no right, license, or interest in or to any Licensed Patent does or shall extend to the Acquirer by reason of the Change of Control transaction, including any rights as to any past, present or future product or service of the Acquirer, except for the rights and license granted to the Acquirer in connection with the Broadcom Licensed Products of the Surviving Broadcom Entity and Surviving Broadcom Affiliates. As used herein, a "Change of Control" means a transaction or series of related transactions in which Broadcom consolidates or merges with or into a Third Party, or sells or transfers all or substantially all of its assets to a Third Party, if the holders of Voting Power of Broadcom as constituted immediately prior to the transaction or series of related transactions will hold, immediately after the transaction or series of related transactions, less than fifty (50%) of the Voting Power of the surviving Person.

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ARTICLE VII – REPRESENTATIONS AND WARRANTIES; INDEMNITY; LIMITATION OF LIABILITY

7.1 Representations and Warranties; Disclaimer.

(a) Each of the parties hereto represents and warrants that (i) it has the right and authority to enter into this Agreement and perform and discharge its obligations hereunder, and (ii) it has not entered into and is not subject to any agreement or obligation that conflicts with this Agreement or the performance of its obligations under this Agreement.

(b) Subject to the Section of Exhibit B (Disclosure Schedule) corresponding to the relevant subclause of this Section 7.1(b), MIPS represents and warrants that (i) Exhibit A sets forth a complete and accurate list of all Patents owned or purported to be owned by MIPS or any of its Affiliates or that have been filed or issued by or in the name of MIPS or any of its Affiliates, (ii) it or one of its Affiliates is the sole and exclusive owner of the Listed Patents, including all rights to recover for alleged infringement of the Listed Patents, (iii) it has the right to grant releases, covenants and licenses with respect to the Listed Patents of the full scope set forth herein and, to its knowledge, there are no Licensed Patents other than the Listed Patents; (iv) no payment of consideration to or consent by any Third Party is required for the covenants, releases and licenses granted herein; (v) neither it nor any of its Affiliates has assigned or otherwise transferred any of its ownership or exclusive rights to any Patent after January 1, 2011 that would otherwise constitute a Licensed Patent under this Agreement if such ownership or exclusive rights had been retained by MIPS or its Affiliate; and (vi) the Affiliates of MIPS as of the Effective Date are listed in Exhibit C and, as of the Effective Date, there is no other Person that directly or indirectly Controls, is Controlled by or is under common Control with MIPS or any of its Affiliates.

(c) MIPS represents and warrants that neither MIPS nor any of its Affiliates, in anticipation of this Agreement participated in any transaction or series of transactions where the result of such transaction(s) is (or was) to avoid extending to Broadcom or its Affiliates the license rights and covenants set forth in this Agreement that Broadcom and its Affiliates otherwise would have enjoyed.

(d) Nothing in this Agreement shall be construed as: (i) requiring the filing of any patent application, the securing of any patent, or the maintaining of any patent in force; (ii) a warranty or representation as to the validity, enforceability, value, or scope of any Patent or other intellectual property right; (iii) a warranty or representation that any manufacture, sale, offering to sell, lease, use, importation, or other disposal of any product, software, or service will not infringe or will be free from infringement of any Patents or other intellectual property rights of any Third Party; or (iv) an agreement to bring or prosecute actions or suits against any Third Party for infringement.

(e) EXCEPT FOR THE EXPRESS WARRANTIES SET FORTH IN THIS AGREEMENT, THE PARTIES MAKE NO REPRESENTATIONS OR WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, EITHER IN FACT OR BY OPERATION OF LAW, BY STATUTE OR OTHERWISE AND HEREBY DISCLAIM ANY

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AND ALL WARRANTIES, INCLUDING ANY AND ALL WARRANTIES OF TITLE, QUIET ENJOYMENT, NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR PURPOSE, OTHER THAN THOSE EXPRESSLY SET FORTH IN THIS AGREEMENT.

(f) EXCEPT WITH RESPECT TO A BREACH OF SECTION 3.3, 3.5, 3.6 OR 7.1, IN NO EVENT SHALL EITHER PARTY BE LIABLE UNDER THIS AGREEMENT FOR ANY INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING LOST PROFITS, OR FOR ANY OTHER PUNITIVE DAMAGES, WHETHER BASED ON CONTRACT, TORT OR ANY OTHER LEGAL THEORY.

ARTICLE VIII– CONFIDENTIALITY

8.1 Confidentiality.

(a) Absent the express written consent of the other Party and except as expressly provided herein, each Party shall keep the terms of this Agreement strictly confidential and shall not disclose any of the terms of this Agreement to any Third Party.

(b) The Parties recognize that certain disclosures of certain terms of this Agreement may be reasonably necessary for the enjoyment of their rights and the performance of their obligations hereunder, and that such disclosures will not require the other Party's consent. Subject to the terms and conditions herein, the following disclosures are permitted hereunder: (i) disclosures by Broadcom to any Broadcom Customers and Broadcom Suppliers of Broadcom's rights under the Licensed Patents; (ii) disclosures to any [*] of the rights, terms, conditions, obligations and covenants set forth herein with respect to [*]; (iii) disclosures to a Party's auditors, accountants or legal counsel in connection with the engagement of such advisors; and (iv) disclosures to any [*]. In disclosures (ii) and (iv), Article IV shall be redacted (except in the case of an actual permitted assignment of this Agreement under (iv) above). In addition, any disclosure under (ii) or (iv) shall be on a confidential, outside attorneys' eyes basis only unless and until [*]. Prior to and as a condition of making a permitted disclosure to a Third Party, the Party making such disclosure shall obtain or have obtained the written agreement of such Third Party obligating such Third Party to non-disclosure and use restrictions as least as protective as those set forth herein, and ensuring that such Third Party will not disseminate the information disclosed regarding the terms of this Agreement to any subsequent Third Party or use such information for any reason other than the reason for which such information is provided to such Third Party. Notwithstanding the above, in no event shall either Party disseminate the terms of this Agreement to any Third Party that does not reasonably need access to such information.

(c) If either Party is required to disclose this Agreement or any of its terms or provisions by law, order, request, or regulation of a court of competent jurisdiction or other governmental agency such that this Agreement or any of its terms or provisions will be made publicly available, then such disclosing Party shall use reasonable efforts to provide the other Party with reasonable advance written notice thereof and, if possible under the circumstances, an opportunity to object to and to try to prevent such disclosure. If either Party believes that it will be necessary to file a copy of all or a portion of this Agreement with the United States Securities and Exchange Commission ("SEC") or any other governmental agency such that this Agreement

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or any of its terms or provisions will be made publicly available, it shall notify the other Party prior to any such filing, provide the other Party with a copy of what it intends to file with the SEC or other governmental agency before making any such filing, request confidential treatment (or a protective order or the equivalent, as applicable) for such disclosure (or such portions as the parties may mutually agree), and provide the other Party with any responses received from the SEC or governmental agency in respect of its request for confidential treatment (or a protective order or the equivalent, if applicable) and any responses thereto by the first Party. If confidential treatment or a protective order or the equivalent is not available for this entire Agreement, the Parties agree to seek confidential treatment for such provisions that either Party may reasonably request. The application for confidential treatment or protective order must be consistent with the requirements of the Freedom of Information Act, rules of the SEC and other applicable laws, rules, or regulations. In addition, each Party shall inform the other Party if the first Party receives notice that disclosure of the Agreement is being sought under the Freedom of Information Act or any similar foreign law, rule, or regulation and use reasonable efforts to maintain confidential treatment if such disclosure is sought.

(d) The Parties' obligations under this ARTICLE VIII will not apply to any information that is or becomes generally available to the public through no wrongful act or omission on the part of either Party.

(e) All prior communications, correspondence, documents, drafts and other information exchanged in connection with the negotiation of this Agreement shall be governed by the terms of that certain Mutual Non-disclosure Agreement dated June 15, 2012 between MIPS and Broadcom.

ARTICLE IX – MISCELLANEOUS PROVISIONS

9.1 Notices. All notices required or permitted to be given hereunder shall be in writing and shall be delivered by hand, or if dispatched by prepaid air courier or by registered or certified airmail, postage prepaid, addressed as follows:

If to MIPS: Attn: General Counsel
MIPS Technologies, Inc.
955 East Arques Avenue
Sunnyvale, California 94085

If to Broadcom: Attn: Executive Vice President and General Counsel
Broadcom Corporation
5300 California Avenue
Irvine, California 92617

Such notices shall be deemed to have been served when received by addressee or, if delivery is not accomplished by reason of some fault of the addressee, when tendered for delivery. Either party may give written notice of a change of address and, after notice of such

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change has been received, any notice or request shall thereafter be given to such party as above provided at such changed address.

9.2 Governing Law. This Agreement and matters connected with the performance thereof shall be construed, interpreted, applied and governed in all respects in accordance with the laws of the United States of America and the State of California, without reference to conflict of laws principles.

9.3 Jurisdiction. MIPS and Broadcom agree (a) that all disputes and litigation between the parties regarding this Agreement and matters connected with its performance be subject to the exclusive jurisdiction of the federal and state courts located in the Northern District of California, and (b) to submit any disputes, matters of interpretation, or enforcement actions arising with respect to the subject matter of this Agreement exclusively to these courts. The parties hereby waive any challenge to the jurisdiction or venue of these courts over these matters. This Section 9.3 shall not be construed as restricting or limiting Broadcom's or any Third Party's ability to immediately assert a release, license, covenant or other defense in any litigation or other proceeding against Broadcom or its Affiliates, or its or their products subject to the releases and other covenants and rights under this Agreement, or the resellers, distributors or customers of such products, regardless of jurisdiction or venue. If any legal action or proceeding relating to this Agreement is brought by either party or its Affiliates against the other party or its Affiliates, the prevailing party shall be entitled to recover reasonable attorneys' fees, costs and disbursements (in addition to any other relief to which the prevailing party may be entitled).

9.4 Bankruptcy. Each party acknowledges that all rights, covenants not to sue and licenses granted under or pursuant to this Agreement are, and shall otherwise be deemed to be, for purposes of Section 365(n) of the United States Bankruptcy Code (the "Bankruptcy Code"), licenses of rights to "intellectual property" as defined under Section 101(56) of the Bankruptcy Code. Each party acknowledges that if such party, as a debtor in possession or a trustee-in-bankruptcy in a case under the Bankruptcy Code, rejects this Agreement, the other party may elect to retain its rights under this Agreement as provided in Section 365(n) of the Bankruptcy Code. Each party irrevocably waives all arguments and defenses arising under 11 U.S.C. 365(c)(1) or successor provisions to the effect that applicable law excuses the party, other than the debtor, from accepting performance from or rendering performance to an entity other than the debtor or debtor in possession as a basis for opposing assumption of the Agreements by the other party in a case under Chapter 11 of the Bankruptcy Code to the extent that such consent is required under 11 U.S.C. § 365(c)(1) or any successor statute.

9.5 Severability. If any provision or portion of a provision of this Agreement is held by a court of competent jurisdiction to be unenforceable or invalid under any applicable statute or rule of law, such court is authorized to modify such provision to the minimum extent necessary to make it enforceable and valid, or eliminate such provision if such modification is not possible, and the remaining provisions or portions of provisions of this Agreement shall in no way be affected or impaired thereby. To the extent a court refuses to give effect to the prior sentence, the parties agree to negotiate in good faith an enforceable substitute provision for any invalid or unenforceable provision or portion of a provision that most nearly achieves the intent of such provision or portion, and the remaining provisions or portions of provisions of this Agreement shall in no way be affected or impaired thereby.

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9.6 Entire Agreement. Each party represents and warrants that no promise, inducement, or agreement not expressly set forth herein has been made in connection with this Agreement. This Agreement is an integrated document representing the entire understanding between the parties with respect to the subject matter hereof. The parties agree that this Agreement (including its Exhibits) supersedes and supplants all prior or contemporaneous agreements, proposal, or understandings, whether written or oral, between them with respect to the same subject matter; provided, however, that the MIPS Technology Licenses, as amended by Attachments 1, 2 and 3, will remain in full force and effect as separate agreements between the parties. For the avoidance of doubt, all purchase, supply and license agreements between MIPS and Broadcom shall remain in full force and effect in accordance with their terms.

9.7 Modification; Waiver. This Agreement may not be modified, amended, supplemented, or repealed except by written agreement executed by duly authorized representatives of the parties, expressly stating that it is the intention of the parties to modify this Agreement. No waiver of, or failure of a party to object to, or failure of a party to take affirmative action with respect to any default, term, or condition of this Agreement, or any breach thereof, shall be deemed to imply or constitute a waiver of any other like default, term, or condition of this Agreement or subsequent breach thereof; nor shall any partial exercise of any right or power preclude any further exercise thereof or the exercise of any other right or power arising from any breach by a party.

9.8 Construction. This Agreement shall be construed in all respects as jointly drafted and shall not be construed, in any way, against either party on the ground that the party or its counsel drafted this Agreement. As used in this Agreement, the words "include" and "including," and variations thereof, will not be deemed to be terms of limitation, but rather will be deemed to be followed by the words "without limitation." The headings in this Agreement are for convenience only, and shall in no way limit, alter of effect the meaning of this Agreement.

9.9 Advice of Counsel. Each party warrants to the other that it has carefully read this Agreement, knows its contents, and has freely and voluntarily executed it without any duress or undue influence on the part of the other party. Each party, by execution of this Agreement, represents that such party has reviewed each term of this Agreement with such party's legal counsel and that such party will not deny the validity of any term of this Agreement on lack of advice of counsel. Each party acknowledges that such party has been represented by independent counsel of that party's choice throughout all negotiations preceding the execution of this Agreement, and that such party has executed this Agreement with the consent, and upon the advice, of such independent counsel.

9.10 Counterparts. This Agreement may be executed in counterparts or duplicate originals, both of which shall be regarded as one and the same instrument, and which shall be the official and governing version in the interpretation of this Agreement. This Agreement may be executed by facsimile or .pdf signatures and such signatures shall be deemed to bind each party as if they were original signatures.

[*Remainder of Page Intentionally Blank*]

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Exhibit 10.40

SIGNATURE PAGE
TO
BROADCOM/MIPS LICENSE AGREEMENT

IN WITNESS WHEREOF, the parties hereto have caused this Agreement to be signed below by their respective duly authorized officers.

MIPS TECHNOLOGIES, INC.	**BROADCOM CORPORATION**
By: /s/ SANDEEP VIJ	By: /s/ SCOTT McGREGOR
Name: Sandeep Vij	Name: Scott McGregor
Title: CEO	Title: CEO
Date: June 29, 2012	Date: June 29, 2012

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Exhibit A:
Listed Patents

Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
US	Granted	12/985680	1/6/2011	8209522	6/26/2012	System and Method for Extracting Fields from Packets having Fields Spread over more than One Register
US	Granted	12/576942	10/9/2009	8190865	5/29/2012	Instruction Encoding For System Register Bit Set and Clear {amended from} Instruction encoding for set/clear of a single bit in any coprocessor register
US	Granted	11/943751	11/21/2007	8190665	5/29/2012	Random Cache Line Refill Order
US	Granted	11/557005	11/6/2006	8185879	5/22/2012	External Trace Synchronization via Periodic Sampling
US	Granted	12/506153	7/20/2009	8185717	5/22/2012	Apparatus and Method for Profiling Software Performance on a Processor with Non-Unique Virtual Addresses
US	Granted	11/279914	4/17/2006	818100	5/15/2012	Method and Apparatus for Binding Shadow Registers to Vectored Interrupts
US	Granted	11/284069	11/21/2005	8171262	5/1/2012	Method and Apparatus for Clearing Hazards Using Jump Instructions
US	Granted	12/684564	1/8/2010	8151268	4/3/2012	Multithreading Microprocessor with Optimized Thread Scheduler for Increasing Pipeline Utilization Efficiency
US	Granted	11/517569	9/8/2006	8151093	4/3/2012	Software Programmable Hardware State Machines
US	Granted	12/605201	10/23/2009	8145884	3/27/2012	Apparatus, Method and Instruction for Initiation of Concurrent Instruction Streams in a Multithreading Microprocessor
US	Granted	11/442696	5/25/2006	8145882	3/27/2012	Apparatus and Method for Processing Template Based User Defined Instructions {f.k.a.} Apparatus and Method to Facilitate the Processing of Template Based User Defined Instructions
US	Granted	11/859198	9/21/2007	8131941	3/6/2012	Support for Multiple Coherence Domains
US	Granted	11/684156	3/9/2007	8103987	1/24/2012	System and Method for Managing the Design and Configuration of an Integrated Circuit Semiconductor Design
US	Granted	12/649132	12/29/2009	8081645	12/20/2011	Context Sharing Between A Streaming Processing Unit (SPU) and A Packet Management (PMU) In A Packet Processing Environment {f.k.a.} Method and Apparatus for Optimizing Selection of Available Contexts for Packet Processing in Multi-Stream Packet Processing
US	Granted	12/911392	10/25/2010	8078806	12/13/2011	Microprocessor with Improved Data Stream Prefetching
US	Granted	11/640491	12/18/2006	8078486	12/13/2011	Conditional Move Instruction Formed Into One Decoded Instruction to be Graduated and Another Decoded Instruction to be Invalidated {f.k.a.} Twice Issued Conditional Move Instruction, and Applications Thereof
US	Granted	12/185594	8/4/2008	8077734	12/13/2011	Method and Apparatus for Predicting Characteristics of Incoming Data Packets to Enable Speculative Processing to Reduce Processor Latency
US	Granted	12/480414	6/8/2009	8074058	12/6/2011	Providing Extended Precision in SIMD Vector Arithmetic Operations
US	Granted	11/838648	8/14/2007	8069354	11/29/2011	Power Management for System Having One or More Integrated Circuits
US	Granted	12/000413	12/12/2007	8051320	11/1/2011	Clock Ratio Controller for Dynamic Voltage and Frequency Scaled Digital Systems, and Applications Thereof
US	Granted	12/557421	9/10/2009	8037253	10/11/2011	Method and Apparatus for Global Ordering to Insure Latency Independent Coherence
US	Granted	11/515723	9/6/2006	8032734	10/4/2011	Coprocessor Load Data Queue for Interfacing an Out-Of-Order Execution Unit with an In-Order Coprocessor {f.k.a.}

						Coprocessor Interface Unit for a Processor, and Applications Thereof
US	Granted	12/021110	1/28/2008	8024539	9/20/2011	Virtual Processor Based Security for On-Chip Memory, and Applications Thereof
US	Granted	11/949418	12/3/2007	8024393	9/20/2011	Processor with Improved Accuracy for Multiply-Add Operations
US	Granted	12/047257	3/12/2008	8001283	8/16/2011	Efficient, Scalable and High Performance Mechanism for Handling IO Requests
US	Granted	11/532523	9/16/2006	7990989	8/2/2011	Transaction Selector Employing Transaction Queue Group Priorities in Multi-Port Switch
US	Granted	12/477059	6/2/2009	7969186	6/28/2011	Apparatus and Method for Forming a Mixed Signal Circuit with Fully Customizable Analog Cells and Programmable Interconnect
US	Granted	11/532522	9/16/2006	7961745	6/14/2011	Bifurcated Transaction Selector Supporting Dynamic Priorities in Multi-Port Switch

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Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
US	Granted	12/432227	4/28/2009	7926062	4/12/2011	Interrupt and Exception Handling for Multi-Streaming Digital Processors
US	Granted	12/348181	1/2/2009	7925864	4/12/2011	Method and Apparatus for Binding Shadow Registers to Vectored Interrupts
US	Granted	12/495375	6/30/2009	7925859	4/12/2011	Three-Tiered Translation Lookaside Buffer Hierarchy in a Multithreading Microprocessor
US	Granted	11/976713	10/26/2007	7917882	3/29/2011	Automated Digital Circuit Design Tool that Reduces or Eliminates Adverse Timing Constraints Due to an Inherent Clock Signal Skew, and Applications Thereof
US	Granted	11/963503	12/21/2007	7917699	3/29/2011	Apparatus and Method for Controlling the Exclusivity Mode of a Level-Two Cache
US	Granted	10/193682	7/12/2002	7911952	3/22/2011	Interface with Credit-Based Flow Control and Sustained Bus Signals
US	Granted	12/274104	11/19/2008	7900207	3/1/2011	Interrupt and Exception Handling for Multi-Streaming Digital Processors
US	Granted	12/421268	4/9/2009	7899993	3/1/2011	Microprocessor Having a Power-Saving Instruction Cache Way Predictor and Instruction Replacement Scheme
US	Granted	12/544167	8/19/2009	7895423	2/22/2011	Method for Extracting Fields from Packets having Fields Spread over more than One Register {as amended}
US	Granted	11/747666	5/11/2007	7886150	2/8/2011	System Debug and Trace System and Method, and Applications Thereof
US	Granted	10/923584	8/20/2004	7886129	2/8/2011	Configurable Co-processor Interface
US	Granted	11/552764	10/25/2006	7877481	1/25/2011	Method and Apparatus for Overflowing Data Packets to a Software-Controlled Memory when they do not Fit into a Hardware-controlled Memory
US	Granted	11/272718	11/15/2005	7873820	1/18/2011	Processor Utilizing a Loop Buffer to Reduce Power Consumption
US	Granted	10/956498	10/1/2004	7873810	1/18/2011	Microprocessor Instruction Using Address Index Values to Enable Access of a Virtual Buffer in Circular Fashion
US	Granted	11/330916	1/11/2006	7870553	1/11/2011	Symmetric Multiprocessor Operating System for Execution on Non-Independent Lightweight Thread Contexts
US	Granted	11/616539	12/27/2006	7865647	1/4/2011	Efficient Resource Arbitration
US	Granted	11/410146	4/25/2006	7860911	12/28/2010	Extended Precision Accumulation
US	Granted	11/051978	2/4/2005	7853777	12/14/2010	Instruction/Skid Buffers in a Multithreading Microprocessor That Store Dispatched Instructions to Avoid Re-Fetching Flushed Instructions { as amended } Instruction/Skid Buffers in a Multithreading Microprocessor
US	Granted	11/313272	12/20/2005	7849297	12/7/2010	Software Emulation of Directed Exceptions in a Multithreading Processor
US	Granted	11/616558	12/27/2006	7840874	11/23/2010	Speculative Cache Tag Evaluation
US	Granted	11/330915	1/11/2006	7836450	11/16/2010	Symmetric Multiprocessor Operating System for Execution on Non-Independent Lightweight Thread Contexts
US	Granted	12/185587	8/4/2008	7822943	10/26/2010	Microprocessor with Improved Data Stream Prefetching
US	Granted	11/702659	2/6/2007	7793077	9/7/2010	Alignment and Ordering of Vector Elements for Single Instruction Multiple Data Processing
US	Granted	11/684205	3/9/2007	7774723	8/10/2010	Protecting Trade Secrets During the Design and Configuration of an Integrated Circuit Semiconductor Design
US	Granted	11/681610	3/2/2007	7774549	8/10/2010	Horizontally-Shared Cache Victims in Multiple Core Processors
US	Granted	11/532521	9/16/2006	7773621	8/10/2010	Transaction Selector Employing Round-Robin Apparatus Supporting Dynamic Priorities in Multi-Port Switch

US	Granted	11/445518	6/2/2006	7770156	8/3/2010	Dynamic Selection of the Best Compression Algorithm for Trace Data
US	Granted	11/767261	6/22/2007	7769958	8/3/2010	Avoiding Livelock Using Intervention Messages in Multiple Core Processors
US	Granted	11/767225	6/22/2007	7769957	8/3/2010	Preventing Writeback Race in Multiple Core Processors
US	Granted	11/566870	12/5/2006	7765554	7/27/2010	Context Selection and Activation Mechanism for Activating one of a Group of Inactive Contexts in a Processor Core for Servicing Interrupts
US	Granted	10/921077	8/18/2004	7765546	7/27/2010	Interstream Control and Communications for Multi-Streaming Digital Processors
US	Granted	11/532520	9/16/2006	7760748	7/20/2010	Transaction Selector Employing Barrel-Incrementer-Based Round-Robin Apparatus Supporting Dynamic Priorities in Multi-Port Switch
US	Granted	11/051980	2/4/2005	7752627	7/6/2010	Leaky-Bucket Thread Scheduler in a Multithreading Microprocessor

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Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
US	Granted	10/637006	8/8/2003	7747989	6/29/2010	Virtual Machine Coprocessor Facilitating Dynamic Compilation
US	Granted	12/104308	4/16/2008	7747840	6/29/2010	Latest Producer Tracking in Out-of-Order Processor
US	Granted	11/868429	10/5/2007	7739484	6/15/2010	Method and Apparatus for Saving and Restoring Processor Register Values and Allocating and Deallocating Stack Memory
US	Granted	11/767247	6/22/2007	7739455	6/15/2010	Avoiding Livelock Using a Cache Manager in Multiple Core Processors
US	Granted	11/261655	10/31/2005	7734901	6/8/2010	Processor Core and Method for Managing Program Counter Redirection in an Out-of-Order Processor Pipeline
US	Granted	11/615964	12/23/2006	7730291	6/1/2010	Symmetric Multiprocessor Operating System for Execution on Non-Independent Lightweight Thread Contexts
US	Granted	11/615963	12/23/2006	7725697	5/25/2010	Symmetric Multiprocessor Operating System for Execution on Non-Independent Lightweight Thread Contexts
US	Granted	11/615960	12/23/2006	7725689	5/25/2010	Symmetric Multiprocessor Operating System for Execution on Non-Independent Lightweight Thread Contexts
US	Granted	11/806845	6/4/2007	7724261	5/25/2010	Processor Having a Compare Extension of an Instruction Set Architecture
US	Granted	11/391716	3/28/2006	7721127	5/18/2010	Multithreaded Dynamic Voltage-Frequency Scaling Microprocessor
US	Granted	11/336938	1/23/2006	7721075	5/18/2010	Conditional Branch Execution in a Processor Having a Write-Tie Instruction and a Data Mover Engine that Associates Register Addresses with Memory Addresses
US	Granted	11/336937	1/23/2006	7721074	5/18/2010	Conditional Branch Execution in a Processor Having a Read-Tie Instruction and a Data Mover Engine that Associates Register Addresses with Memory Addresses
US	Granted	11/336923	1/23/2006	7721073	5/18/2010	Conditional Branch Execution in a Processor Having a Data Mover Engine That Associates Register Addresses with Memory Addresses
US	Granted	11/362764	2/28/2006	7721071	5/18/2010	System and Method for Propagating Operand Availability Identifiers with Instructions Through a Pipeline in an Out-of-Order Processor (as amended)
US	Granted	11/277293	3/23/2006	7715410	5/11/2010	Queuing System for Processors in Packet Routing Operations
US	Granted	11/261654	10/31/2005	7711934	5/4/2010	Processor Core and Method for Managing Branch Misprediction in an Out-of-Order Processor Pipeline
US	Granted	10/954988	9/30/2004	7711931	5/4/2010	Synchronized Storage Providing Multiple Synchronization Semantics
US	Granted	09/836541	4/18/2001	7711926	5/4/2010	Mapping System and Method for Instruction Set Processing
US	Granted	09/788684	2/21/2001	7711763	5/4/2010	Microprocessor Instructions for Performing Polynomial Arithmetic Operations
US	Granted	11/278874	4/6/2006	7707391	4/27/2010	Methods and Apparatus for Improving Fetching and Dispatch of Instructions in Multithreaded Processors
US	Granted	10/698061	10/31/2003	7707389	4/27/2010	Multi-ISA Instruction Fetch Unit for a Processor, and Applications Thereof (as amended)
US	Granted	11/537584	9/29/2006	7702055	4/20/2010	Apparatus and Method for Tracing Processor State From Multiple Clock Domains
US	Granted	11/674924	2/14/2007	7698533	4/13/2010	Configurable Coprocessor Interface
US	Granted	10/929102	8/27/2004	7694304	4/6/2010	Mechanisms for Dynamic Configuration of Virtual Processor Resources
US	Granted	11/191258	7/27/2005	7681014	3/16/2010	Multithreading Instruction Scheduler Employing Thread Group Priorities

US	Granted	11/615965	12/23/2006	7676664	3/9/2010	Symmetric Multiprocessor Operating System for Execution on Non-Independent Lightweight Thread Contexts
US	Granted	11/949603	12/3/2007	7676660	3/9/2010	System, Method, and Computer Program Product for Conditionally Suspending Issuing Instruction of a Thread
US	Granted	11/051998	2/4/2005	7664936	2/16/2010	Prioritizing Thread Selection Partly Based on Stall Likelihood Providing Status Information of Instruction Operand Register Usage at Pipeline Stages
US	Granted	11/463950	8/11/2006	7664920	2/16/2010	Microprocessor with Improved Data Stream Prefetching
US	Granted	11/278747	4/5/2006	7661112	2/9/2010	Methods and Apparatus for Managing a Buffer of Events in the Background
US	Granted	11/620362	1/5/2007	7660969	2/9/2010	Multithreading Instruction Scheduler Employing Thread Group Priorities
US	Granted	11/051979	2/4/2005	7657891	2/2/2010	Multithreading Microprocessor with Optimized Thread Scheduler for Increasing Pipeline Utilization Efficiency
US	Granted	11/087070	3/22/2005	7657883	2/2/2010	Instruction Dispatch Scheduler Employing Round-Robin Apparatus Supporting Multiple Thread Priorities for Use in Multi-threading Micro-processor

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US	Granted	11/505869	8/18/2006	7657708	2/2/2010	Methods for Reducing Data Cache Access Power in a Processor, and Applications Thereof
US	Granted	11/676541	2/20/2007	7650605	1/19/2010	Method and Apparatus for Implementing Atomicity of Memory Operations in Dynamic Multi-Streaming Processors
US	Granted	11/505865	8/18/2006	7650465	1/19/2010	Processor Having a Micro Tag Array That Reduces Data Cache Access Power, and Applications Thereof
US	Granted	09/881628	6/13/2001	7649901	1/19/2010	Method and Apparatus for Optimizing Selection of Available Contexts for Packet Processing in Multi-Stream Packet Processing
US	Granted	11/515720	9/6/2006	7647475	1/12/2010	System for Synchronizing an In-Order Co-processor with an Out-of-Order Processor Using a Co-processor Interface Store Data Queue (as amended)
US	Granted	12/187631	8/7/2008	7644319	1/5/2010	Trace Control From Hardware and Software
US	Granted	11/380924	4/29/2006	7644307	1/5/2010	Functional Validation of a Packet Management Unit
US	Granted	10/783960	2/20/2004	7644237	1/5/2010	Latency Independent Coherence Protocol
US	Granted	12/173560	7/15/2008	7636836	12/22/2009	Fetch and Dispatch Decoupling Mechanism for Multi-Streaming Processors
US	Granted	10/279210	10/22/2002	7634638	12/15/2009	Instruction Encoding for System Register Bit Set and Clear
US	Granted	11/214466	8/29/2005	7634619	12/15/2009	Method and Apparatus for Redirection of Operations Between Interfaces
US	Granted	11/087064	3/22/2005	7631130	12/8/2009	Barrel-Incrementer-Based Round-Robin Apparatus and Instruction Dispatch Scheduler Employing Same for Use in Multithreading Microprocessor
US	Granted	11/442695	5/25/2006	7627794	12/1/2009	Apparatus and Method for Discrete Test Access Control of Multiple Cores
US	Granted	11/107492	4/14/2005	7627770	12/1/2009	Apparatus and Method for Automatic Low Power Mode Invocation in a Multi-Threaded Processor
US	Granted	11/257381	10/24/2005	7620832	11/17/2009	Method and Apparatus for Masking a Microprocessor Execution Signature
US	Granted	11/644001	12/22/2006	7617388	11/10/2009	Virtual Instruction Expansion Using Parameter Selector Defining Logic Operation on Parameters for Template Opcode Substitution
US	Granted	12/348847	1/5/2009	7613966	11/3/2009	HYPERJTAG System Including Debug Probe, On-Chip Instrumentation and Protocol
US	Granted	11/051997	2/4/2005	7613904	11/3/2009	Interfacing External Thread Prioritizing Policy Enforcing Logic with Customer Modifiable Register to Processor Internal Scheduler
US	Granted	10/928746	8/27/2004	7610473	10/27/2009	Apparatus, Method and Instruction for Initiation of Concurrent Instruction Streams in a Multithreading Microprocessor
US	Granted	11/107489	4/14/2005	7600135	10/6/2009	Apparatus and Method for Software Specified Power Management Performance Using Low Power Virtual Threads
US	Granted	11/567290	12/6/2006	7600100	10/6/2009	Instruction Encoding for System Register Bit Set and Clear
US	Granted	09/788670	2/21/2001	7599981	10/6/2009	Binary Polynomial Multiplier
US	Granted	10/955231	9/30/2004	7594089	9/22/2009	Smart Memory Based Synchronization Controller for a Multithreaded Microprocessor SoC
US	Granted	11/545706	10/11/2006	7594079	9/22/2009	Data Cache Virtual Hint Way Prediction, and Applications Thereof
US	Granted	11/279136	4/10/2006	7581091	8/25/2009	System and Method for Extracting Fields from Packets Having Fields Spread Over More Than One Register
US	Granted	11/272719	11/15/2005	7562191	7/14/2009	Microprocessor Having a Power-Saving Instruction Cache Way Predictor and Instruction Replacement Scheme

US	Granted	11/075041	3/8/2005	7558939	7/7/2009	Three Tiered Translation Lookaside Buffer Hierarchy in a Multithreading Microprocessor
US	Granted	09/977089	10/12/2001	7552261	6/23/2009	Configurable Prioritization of Core Generated Interrupts
US	Granted	11/360338	2/23/2006	7551626	6/23/2009	Queuing System for Processors in Packet Routing Operations
US	Granted	11/337440	1/24/2006	7546443	6/9/2009	Providing Extended Precision in SIMD Vector Arithmetic Operations
US	Granted	11/764137	6/15/2007	7543207	6/2/2009	Full Scan Solution for Latched-Based Design
US	Granted	11/463954	8/11/2006	7533220	5/12/2009	Microprocessor with Improved Data Stream Prefetching
US	Granted	11/552640	10/25/2006	7529915	5/5/2009	Context Switching Processor with Multiple Context Control Register Sets Including Write Address Register Identifying Destination Register for Waiting Context to Store Returned Data From External Source
US	Granted	11/876442	10/22/2007	7529907	5/5/2009	Method and Apparatus for Improved Computer Load and Store Operations

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US	Granted	11/463939	8/11/2006	7512740	3/31/2009	Microprocessor with Improved Data Stream Prefetching
US	Granted	11/636462	12/11/2006	7509480	3/24/2009	Boundary Address Registers for Selection of ISA Mode
US	Granted	11/549418	10/13/2006	7509459	3/24/2009	Microprocessor with Improved Data Stream Prefetching
US	Granted	11/003120	12/3/2004	7509456	3/24/2009	Apparatus and Method for Discovering a Scratch Pad Memory Configuration
US	Granted	11/611064	12/14/2006	7509447	3/24/2009	Barrel-Incrementer-Based Round-Robin Apparatus and Instruction Dispatch Scheduler Employing Same for Use in Multithreading Microprocessor
US	Granted	11/086258	3/22/2005	7506140	3/17/2009	Return Data Selector Employing Barrel-Incrementer-Based Round Robin Apparatus
US	Granted	11/549413	10/13/2006	7506106	3/17/2009	Microprocessor with Improved Data Stream Prefetching
US	Granted	09/602279	6/23/2000	7502876	3/10/2009	Background Memory Manager That Determines if Data Structures Fit in Memory with Memory State Transactions Map
US	Granted	11/272737	11/15/2005	7496771	2/24/2009	Processor Accessing a Scratch Pad On-Demand to Reduce Power Consumption
US	Granted	11/087063	3/22/2005	7490230	2/10/2009	Fetch Director Employing Barrel-Incrementer-Based Round Robin Apparatus for Use in Multithreading Microprocessor
US	Granted	09/977084	10/12/2001	7487339	2/3/2009	Method and Apparatus for Binding Shadow Registers to Vectored Interrupts
US	Granted	11/668582	1/30/2007	7487332	2/3/2009	Method and Apparatus for Binding Shadow Registers to Vectored Interrupts
US	Granted	11/463957	8/11/2006	7480769	1/20/2009	Microprocessor with Improved Data Stream Prefetching
US	Granted	11/026324	12/29/2004	7475303	1/6/2009	HYPERJTAG System Including Debug Probe, On-Chip Instrumentation and Protocol
US	Granted	11/277101	3/21/2006	7467385	12/16/2008	Interrupt and Exception Handling for Multi-Streaming Digital Processors
US	Granted	10/929097	8/27/2004	7424599	9/9/2008	Apparatus, Method and Instruction for Software Management of Multiple Computational Contexts in a Multithreaded Microprocessor
US	Granted	11/330914	1/11/2006	7418585	8/26/2008	Symmetric Multiprocessor Operating System for Execution on Non-Independent Lightweight Thread Contexts
US	Granted	09/935446	8/22/2001	7415531	8/19/2008	Prediction of Packet Flow, Packet Header and Packet Payload
US	Granted	11/676242	2/16/2007	7412630	8/12/2008	Trace Control From Hardware and Software
US	Granted	11/539322	10/6/2006	7406586	7/29/2008	Fetch and Dispatch Disassociation Apparatus for Multi-Streaming Processors
US	Granted	09/637500	8/11/2000	7401205	7/15/2008	High Performance RISC Instruction Set Digital Signal Processor Having Circular Buffer Control and Looping Instuction Commands (as amended)
US	Granted	11/365280	2/28/2006	7386701	6/10/2008	Prefetching Hints
US	Granted	10/684350	10/10/2003	7376954	5/20/2008	Mechanism for Assuring Quality of Service for Programs Executing on a Multithread Processor
US	Granted	11/485959	7/14/2006	7370178	5/6/2008	Method for Latest Producer Tracking in an Out-of-Order Processor, and Applications Thereof
US	Granted	09/364512	7/30/1999	7346643	3/18/2008	Processor with Improved Accuracy for Multiply-Add Operations
US	Granted	10/929342	8/27/2004	7321965	1/22/2008	Integrated Mechanism for Suspension and Deallocation of Computational Threads of Execution in a Processor
US	Granted	10/141579	5/9/2002	7318145	1/8/2008	Random Slip Generator
US	Granted	10/956490	10/1/2004	7315937	1/1/2008	Microprocessor Instructions for Efficient Bit Stream Extractions

US	Granted	10/141926	5/10/2002	7310706	12/18/2007	Random Cache Line Refill Order
US	Granted	09/751748	12/29/2000	7287147	10/23/2007	Configurable Coprocessor Interface
US	Granted	10/994827	11/23/2004	7281123	10/9/2007	Restoring Register Values from Stack Memory Using Instruction with Restore Indication Bit and De-allocation Frame Size Stack Pointer Offset
US	Granted	11/278890	4/6/2006	7280548	10/9/2007	Method and Apparatus for Non-Speculative Pre-Fetch Operation in Data Packet Processing
US	Granted	09/592106	6/12/2000	7257814	8/14/2007	Method and Apparatus for Implementing Atomicity of Memory Operations in Dynamic Multi-Streaming Processors
US	Granted	10/255107	9/26/2002	7246287	7/17/2007	Full Scan Solution for Latched-Based Design
US	Granted	09/364786	7/30/1999	7242414	7/10/2007	Processor Having a Compare Extension of an Instruction Set Architecture
US	Granted	09/788683	2/21/2001	7237097	6/26/2007	Partial Bitwise Permutations

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Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
US	Granted	09/595776	6/16/2000	7237093	6/26/2007	Instruction Fetching System in a Multithreaded Processor Utilizing Cache Miss Predictions to Fetch Instructions from Multiple Hardware Streams
US	Granted	09/751747	12/29/2000	7237090	6/26/2007	Configurable Out-of-Order Data Transfer in a Corprocessor Interface
US	Granted	09/894831	6/29/2001	7231551	6/22/2007	Distributed TAP Controller
US	Granted	10/195522	7/16/2002	7225212	5/29/2007	Extended Precision Accumulator
US	Granted	09/662832	9/15/2000	7197625	3/27/2007	Alignment & Ordering of Vector Elements for Single Instruction Multiple Data Processing
US	Granted	11/278901	4/6/2006	7197043	3/27/2007	Method for Allocating Memory Space for Limited Packet Head and/or Tail Growth
US	Granted	11/380925	4/29/2006	7194599	3/20/2007	Configurable Co-Processor Interface
US	Granted	10/449818	5/30/2003	7194582	3/20/2007	Microprocessor with Improved Data Stream Prefetching
US	Granted	09/844669	4/30/2001	7185234	2/27/2007	Trace Control From Hardware and Software
US	Granted	09/921400	8/2/2001	7185183	2/27/2007	Atomic Update of CPO State
US	Granted	09/844271	4/30/2001	7181728	2/20/2007	User-Controlled Trace Records
US	Granted	09/921377	8/2/2001	7181600	2/20/2007	Read-only Access to CPO Registers
US	Granted	09/788685	2/21/2001	7181484	2/20/2007	Extended-Precision Accumulation of Multiplier Output
US	Granted	09/844673	4/30/2001	7178133	2/13/2007	Trace Control Based on a Characteristic of a Processor's Operating State
US	Granted	10/449825	5/30/2003	7177985	2/13/2007	Microprocessor with Improved Data Stream Prefetching
US	Granted	09/844670	4/30/2001	7168066	1/23/2007	Tracing Out-of-Order Load Data
US	Granted	09/927129	8/10/2001	7165257	1/16/2007	Context Selection and Activation Mechanism for Activating One of a Group of Inactive Contexts in a Processor Core for Servicing Interrupts
US	Granted	09/788682	2/21/2001	7162621	1/9/2007	Virtual Instruction Expansion Based on Template and Parameter Selector Information Specifying Sign-Extension or Concatenation
US	Granted	09/591510	6/12/2000	7162615	1/9/2007	Data Transfer Bus Communication Using Single Request to Perform Command and Return Data to Context Associated Destination Registration (Amended)
US	Granted	10/448324	5/28/2003	7159101	1/2/2007	System and Method to Trace High-Performance Multi-Issue Processors
US	Granted	09/223046	12/30/1998	7159100	1/2/2007	Method for Providing Extended Precision in SIMD Vector Arithmetic Operations
US	Granted	09/964827	9/25/2001	7155516	12/26/2006	Method and Apparatus for Overflowing Data Packets to a Software-Controlled Memory when they do not Fit into a Hardware-controlled Memory
US	Granted	09/702112	10/30/2000	7149878	12/12/2006	Changing Instruction Set Architecture Mode by Comparison of Current Instruction Execution Address with Boundary Address Register Values
US	Granted	09/948919	9/7/2001	7139901	11/21/2006	Extended Instruction Set for a Packet Processing Applications
US	Granted	09/706154	11/3/2000	7139898	11/21/2006	Fetch and Dispatch Disassociation Apparatus for Multi-Streaming Processors
US	Granted	09/844668	4/30/2001	7134116	11/7/2006	External Trace Synchronization via Periodic Sampling
US	Granted	09/804677	3/12/2001	7127586	10/24/2006	Prefetching Hints
US	Granted	09/844671	4/30/2001	7124072	10/17/2006	Program Counter and Data Tracing from a Multi-Issue Processor
US	Granted	09/925314	8/10/2001	7107439	9/12/2006	Control of Software Decompression through the use of Exceptions Due to Unaligned Instruction Fetch
US	Granted	09/954290	9/11/2001	7082552	7/25/2006	Functional Validation of a Packet Management Unit

US	Granted	09/881934	6/14/2001	7076630	7/11/2006	Method and Apparatus for Allocating and De-allocating Consecutive Blocks of Memory in Background Memory Management
US	Granted	09/844672	4/30/2001	7069544	6/27/2006	Dynamic Selection of a Compression Algorithm for Trace Data
US	Granted	09/850195	5/8/2001	7065675	6/20/2006	System and Method for Speeding Up EJTAG Block Data Transfers
US	Granted	09/933934	8/20/2001	7065096	6/20/2006	Method for Allocating Memory Space for Limited Packet Head and/or Tail Growth
US	Granted	09/924755	8/7/2001	7058065	6/6/2006	Methods and Apparatus for Preventing Undesirable Packet Download with Pending Read/Write Operation in Data Packet Processing
US	Granted	09/737375	12/14/2000	7058064	6/6/2006	Queuing System for Processors in Packet Routing Operations
US	Granted	09/894832	6/29/2001	7055070	5/30/2006	Trace Control Block Implementation and Method

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Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
US	Granted	09/894830	6/29/2001	7043668	5/9/2006	Optimized External Trace Formats
US	Granted	09/586115	6/2/2000	7043467	5/9/2006	Wire-speed Multi-Dimensional Packet Classifier
US	Granted	09/900393	7/5/2001	7042887	5/9/2006	Method and Apparatus for Non-Speculative Pre-Fetch Operation in Data Packet Processing
US	Granted	09/799610	3/7/2001	7039060	5/2/2006	System and Method for Extracting Fields from Packets Having Fields Spread Over More Than One Register
US	Granted	09/706157	11/3/2000	7035998	4/25/2006	Clustering Stream and/or Instruction Queues for Multi-Streaming Processors
US	Granted	09/616385	7/14/2000	7035997	4/25/2006	Methods and Apparatus for Improving Fetching and Dispatch of Instructions in Multithreaded Processor
US	Granted	09/608750	6/30/2000	7032226	4/18/2006	Methods and Apparatus for Managing a Buffer of Events in the Background
US	Granted	09/312302	5/14/1999	7020879	3/28/2006	Interrupt and Exception Handling for Multi-Streaming Digital Processors
US	Granted	10/186290	6/27/2002	7017025	3/21/2006	Mechanism for Proxy Management of Multiprocessor Virtual Memory
US	Granted	10/186330	6/27/2002	7003630	2/21/2006	Mechanism for Proxy Management of Multiprocessor Storage Hierarchies
US	Granted	10/238993	9/6/2002	7000095	2/14/2006	Method and Apparatus for Clearing Hazards Using Jump Instructions
US	Granted	09/577238	5/23/2000	6996596	2/7/2006	Flush-to-nearest mode to improve floating-point accuracy over existing flush-to-zero mode
US	Granted	10/274424	10/18/2002	6987405	1/17/2006	Apparatus and Method for Generating Multi-Phase Signals with Digitally Controlled Trim Capacitors
US	Granted	09/894812	6/28/2001	6976178	12/13/2005	Inhibition Feature to System for Prediction and Control of Power Consumption in Digital Systems
US	Granted	10/135004	4/26/2002	6961819	11/1/2005	Method and Apparatus for Redirection of Operations Between Interfaces
US	Granted	09/363637	7/30/1999	6912559	6/28/2005	System and Method for Improving the Accuracy of Reciprocal and Reciprocal Square Root Operations Performed by a Floating Point Unit
US	Granted	10/159818	5/31/2002	6883156	4/19/2005	Apparatus and Method for Relative Position Annotation of Standard Cell Components to Facilitate Datapath Design
US	Granted	10/278537	10/22/2002	6836833	12/28/2004	Apparatus and Method for Discovering a Scratch Pad Memory Configuration
US	Granted	09/882285	6/18/2001	6826681	11/30/2004	Method and Apparatus for Saving and Restoring Processor Register Values and Allocating and Deallocating Stack Memory
US	Granted	10/071547	2/8/2002	6789100	9/7/2004	Interstream Control and Communications for Multi-Streaming Digital Processors
US	Granted	09/753239	12/29/2000	6754804	6/22/2004	Coprocessor Interface Transferring Multiple Instructions Simultaneiously Along with Issue Path Designation and/or Issue Order Designation for the Instructions
US	Granted	09/818946	3/28/2001	6742165	5/25/2004	System, Method and Computer Program Product for Web-Based Integrated Circuit Design
US	Granted	09/364789	7/30/1999	6732259	5/4/2004	Processor Having a Conditional Branch Extension of an Instruction Set Architecture
US	Granted	09/318551	5/27/1999	6732208	5/4/2004	Low Latency System Bus Interface For Multi-Master Processing Environments
US	Granted	09/905185	7/13/2001	6728859	4/27/2004	Programmable Page Table Access
US	Granted	09/364787	7/30/1999	6714197	3/30/2004	Processor Having an Arithmetic Extension of an Instruction Set Architecture

US	Granted	09/364514	7/30/1999	6697832	2/24/2004	Floating-Point Processor with Improved Intermediate Result Handling
US	Granted	09/863898	5/24/2001	6691221	2/10/2004	Apparatus for Processing Instructions in a Computing System
US	Granted	09/373094	8/12/1999	6681283	1/20/2004	Coherent Data Apparatus for an On-Chip Split Transaction System Bus
US	Granted	09/654064	9/1/2000	6651160	11/18/2003	Register Set Extension for Compressed Instruction Set
US	Granted	09/822783	3/30/2001	6651156	11/18/2003	Mechanism for Extending Properties of Virtual memory Pages Mapped by a TLB
US	Granted	09/822796	3/30/2001	6643759	11/4/2003	Mechanism to Extend Computer Memory Protection Schemes
US	Granted	09/363638	7/30/1999	6631392	10/7/2003	Method and Apparatus for Predicting Floating-Point Exceptions
US	Granted	09/665099	9/20/2000	6625737	9/23/2003	System for Prediction and Control of Power Consumption in Digital Systems

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Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
US	Granted	09/373093	8/12/1999	6604159	8/5/2003	Data Release to Reduce Latency in On-Chip System Bus
US	Granted	09/905180	7/13/2001	6523104	2/18/2003	Mechanism for Programmable Modification of Memory Mapping Granularity
US	Granted	09/373091	8/12/1999	6493776	12/10/2002	Scalable On-Chip System Bus
US	Granted	09/373092	8/12/1999	6490642	12/3/2002	Locked Read/Write on Separate Address/Data Bys Using Write Barrier
US	Granted	09/216017	12/16/1998	6477562	11/5/2002	Prioritized Instruction Scheduling for Multi-Streaming Processors
US	Granted	09/734713	12/13/2000	6448817	9/10/2002	Output-Synchronization Free, High-Fanin Dynamic OR/ NOR Gate
US	Granted	09/517272	3/2/2000	6446171	9/3/2002	Method and Apparatus for Tracking and Update of LRU Algorithm Using Vectors
US	Granted	09/494488	1/31/2000	6430655	8/6/2002	Scratchpad RAM with Cache-Like Access Times
US	Granted	09/544352	4/6/2000	6425076	7/23/2002	Instruction Prediction Based on Filtering
US	Granted	09/373095	8/12/1999	6393500	5/21/2002	Burst-Configurable Data Bus
US	Granted	09/273810	3/22/1999	6389449	5/14/2002	Interstream Control and Communications for Multi-Streaming Digital Processors
US	Granted	09/302246	4/29/1999	6345354	2/5/2002	Register File Access
US	Granted	09/240012	1/27/1999	6292888	9/18/2001	Register Transfer Unit for Electronic Processor
US	Granted	09/263798	3/5/1999	6266758	7/24/2001	Alignment & Ordering of Vector Elements for Single Instruction Multiple Data Processing
US	Granted	09/363635	7/30/1999	6247124	6/12/2001	Apparatus for Processing Instructions in a Computing System
US	Granted	08/982244	12/1/1997	6240488	5/29/2001	Prefetching Hints
US	Granted	09/383401	8/26/1999	6188248	2/13/2001	Output-Synchronization Free, High-Fanin Dynamic OR/ NOR Gate
US	Granted	08/935369	9/22/1997	6092187	7/18/2000	Instruction Prediction Based on Filtering
US	Granted	09/036684	3/9/1998	5978926	11/2/1999	Processor Chip Having On-Chip Circuitry for Generating a Programmable External Clock Signal & for Controlling Data Patterns
US	Granted	08/781851	1/10/1997	5954815	9/21/1999	Apparatus for Processing Instructions in a Computing System
US	Granted	08/947649	10/9/1997	5933650	8/3/1999	Alignment & Ordering of Vector Elements for Single Instruction Multiple Data Processing
US	Granted	08/686363	7/24/1996	5870574	2/9/1999	RISC Processor Having Improved Instruction Fetching Capability & Utilizing Address Bit Precoding for a Segmented Cache Memory
US	Granted	08/947648	10/9/1997	5864703	1/26/1999	Providing Extended Precision in SIMD Vector Arithmetic Operations
US	Granted	08/487240	6/13/1995	5740402	4/14/1998	Conflict Resolution in Interleaved Memory Systems with Multiple Parallel Accesses
US	Granted	08/715246	9/19/1996	5734877	3/31/1998	Processor Chip Having On-Chip Circuitry for Generating a Programmable External Clock Signal & for Controlling Data Patterns
US	Granted	08/410524	3/24/1995	5732242	3/24/1998	Prefetching Hints
US	Granted	08/484313	6/7/1995	5699551	12/16/1997	Two-Level Cache Memory System
US	Granted	08/405622	3/15/1995	5696958	12/9/1997	Method & Apparatus for Reducing Delays Following the Execution of a Branch Instruction in an Instruction Pipeline
US	Granted	08/561914	11/22/1995	5670898	9/23/1997	Low-Power Compact Digital Logic Topology that Facilitates Large Fan-In & High Speed
US	Granted	08/696788	8/14/1996	5632025	5/20/1997	System and Method for Coherency in a Split-Level Data Cache System

US	Granted	08/245983	5/17/1994	5619672	4/8/1997	Precise Translation Lookaside Buffer Error Detection & Shutdown Circuit
US	Granted	08/168744	12/15/1993	5604909	2/18/1997	Apparatus for Processing Instructions in a Computing System
US	Granted	08/449588	5/24/1995	5590294	12/31/1996	Method & Apparatus for Restarting Pipeline Processing
US	Granted	07/951471	9/25/1992	5574877	11/12/1996	TLB With Physical Pages Per Virtual Tag
US	Granted	08/379710	1/27/1995	5572713	11/5/1996	Method & Apparatus For Byte Order Switching in a Computer
US	Granted	08/167005	12/15/1993	5572704	11/5/1996	System and Method for Coherency in a Split-Level Data Cache System
US	Granted	08/391946	2/21/1995	5568630	10/22/1996	Backward Compatible Computer Architecture with Extended Wordsize and Address Space
US	Granted	08/491491	6/16/1995	5568442	10/22/1996	RISC Processor Having Improved Instruction Fetching Capability & Utilizing Address Bit Precoding for a Segmented Cache Memory
US	Granted	08/324861	10/18/1994	5555384	9/10/1996	Optimized Pipeline Operations for Reduced Instruction Set Computers

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Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
US	Granted	08/172684	12/22/1993	5542062	7/30/1996	Two-Level Cache Memory System
US	Granted	08/166969	12/15/1993	5537538	7/16/1996	Debug Mode for a Superscalar RISC Processor
US	Granted	08/168822	12/15/1993	5526504	6/11/1996	Variable Page Size Translation Lookaside Buffer
US	Granted	08/378844	1/26/1995	5524245	6/4/1996	System and Method for Booting Computer for Operation in Either of Two Byte-Order Modes
US	Granted	08/168832	12/15/1993	5510934	4/23/1996	Apparatus for Processing Instructions in a Computing System
US	Granted	08/245200	5/17/1994	5504698	4/2/1996	A Compact Dual Function Adder
US	Granted	08/167006	12/15/1993	5493523	2/20/1996	Mechanism and Method for Integer Divide Involving Pre-Alignment of the Divisor Relative to the Dividend
US	Granted	07/918819	7/22/1992	5491702	2/13/1996	Apparatus for Detecting Any Single Bit Error, Detecting Any Two Bit Error, & Detecting any Three or Four Bit Error in a Group of Four Bits for a 25- or 64-Bit Data Word
US	Granted	08/212377	3/11/1994	5479630	12/26/1995	Hybrid Cache Having Physical-Cache & Virtual-Cache Characteristics & Method for Accessing Same
US	Granted	08/063183	5/17/1993	5450607	9/12/1995	Unified Floating Point and Integer Datapath for a RISC Processor
US	Granted	07/933467	8/21/1992	5317601	5/31/1994	Clock Distribution System for an Integrated Circuit Device
US	Granted	07/956867	10/1/1992	5309382	5/3/1994	Binary Shifter

Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
US	Allowed	12/346652	12/30/2008			Thread Instruction Fetch Based On Prioritized Selection From Plural Round-Robin Outputs For Different Thread States (as amended) FETCH DIRECTOR EMPLOYING BARREL-INCREMENTER-BASED ROUND-ROBIN APPARATUS FOR USE IN MULTITHREADING MICROPROCESSOR
US	Allowed	12/891503	9/27/2010			MICROPROCESSOR WITH DUAL-LEVEL ADDRESS TRANSLATION
US	Pending	10/637005	8/8/2003			Virtual Machine Coprocessor for Accelerating Software Execution
US	Pending	11/388484	3/23/2006			USER INTERFACE FOR FACILITATION OF HIGH LEVEL GENERATION OF PROCESSOR EXTENSIONS
US	Pending	13/161332	6/15/2011			Programmable Memory Address Segments { f.k.a.} Apparatus and Method for Converting Fixed Memory Address Segments Into Programmable Memory Address Segments {as amended} Segmentation Scheme
US	Pending	13/161354	6/15/2011			Apparatus and Method for Hardware Initiation of Emulated Instructions {as amended from} Apparatus and Method for Hardware Initiation of Guest Machine Operations
US	Pending	13/168870	6/24/2011			Apparatus and Method for Accelerated Hardware Page Table Walk {f.k.a.} Method to Reduce the Number of Memory Accesses During a Hardware Page Table Walk
US	Pending	13/328781	12/16/2011			System for Compression of Fixed Width Variables in a CPU Hardware Trace
US	Pending	13/328792	12/16/2011			Vector Register Length Agnostic Single Instruction Multiple Data (SIMD) Architecture

US	Pending	13/358399	1/25/2012	Merged Floating Point Operation Using a Modebit {f.k.a. MADD Fused/Non-Fused Modebit}
US	Pending	13/360319	1/27/2012	MULTITHREADED OPERATION OF A MICROPROCESSOR CACHE {f.k.a.} Power Reduction Instruction Cache in a Multi-Thread Processor Core
US	Pending	13/361441	1/30/2012	Support for Multiple Coherence Domains
US	Pending	13/404350	2/24/2012	Software Programmable Hardware State Machines
US	Pending	13/436654	3/30/2012	APPARATUS AND METHOD FOR GUEST AND ROOT REGISTER SHARING IN A VIRTUAL MACHINE
US	Pending	13/491781	6/8/2012	Shared Register Pool for a Multithreaded Microprocessor
US	Pending	61/562952	11/22/2011	MIPS32 Enhanced VA Scheme
US	Pending	61/562975	11/22/2011	Achieving Glitch-Free Clock Domain Crossing Signals Using Formal Verification, Static Timing Analysis, and Sequential Equivalence Checking

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Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
US	Published	11/121945	5/5/2005			Processor Core and Multiplier That Support Both Vector and Single Value Multiplication
US	Published	11/122004	5/5/2005			Processor Core and Multiplier that Support a Multiply and Difference Operation by Inverting Sign Bits in Booth Recoding
US	Published	11/313296	12/20/2005			Preemptive Multitasking Employing Software Emulation of Directed Exceptions in a Multithreading Processor
US	Published	11/362763	2/28/2006			Compact Linked-List-Based Multi-Threaded Instruction Graduation Buffer
US	Published	11/485960	7/14/2006			Latest Producer Tracking in an Out-of-Order Processor, and Applications Thereof
US	Published	11/529710	9/29/2006			Detection and Prevention of Write-After-Write Hazards, and Applications Thereof
US	Published	11/529728	9/29/2006			Load/Store Unit for a Processor, and Applications Thereof
US	Published	11/530945	9/12/2006			Extended Instruction Set for Packet Processing Applications
US	Published	11/627899	1/26/2007			Systems and Methods for Controlling the Use of Processing Algorithms, and Applications Thereof
US	Published	11/655267	1/19/2007			Synthesized Assertions in a Self-Correcting Processor and Applications Thereof
US	Published	11/670876	2/2/2007			System, Method and Software Application for the Generation of Verification Programs {f.k.a.} Software and Techniques for Generation of Self-Checking Random Programs
US	Published	11/684189	3/9/2007			Remote Interface for Managing the Design and Configuration of an Integrated Circuit Semiconductor Design
US	Published	11/727640	3/27/2007			High-Performance RISC-DSP
US	Published	11/830795	7/30/2007			Apparatus and Method for Evaluating a Free-Running Trace Stream {as amended from} Free-Running Real-Time PDTrace Decoder
US	Published	11/864363	9/28/2007			Speculative Read In a Cache Coherent Microprocessor
US	Published	11/896424	8/31/2007			Low-overhead/Power-Saving Processor Synchronization Mechanism, and Applications Thereof
US	Published	12/058117	3/28/2008			Mechanism for Maintaining Consistency of Data Written by IO Devices
US	Published	12/060204	3/31/2008			Apparatus and Method for Condensing Trace Information in a Multi-Processor System
US	Published	12/060214	3/31/2008			Apparatus and Method for Low Overhead Correlation of Multi-Processor Trace Information
US	Published	12/194936	8/20/2008			Data Cache Way Prediction
US	Published	12/195053	8/20/2008			Data Cache Receive Flop Bypass
US	Published	12/210150	9/12/2008			Methods, Systems and Computer Program Products for Evaluating Electrical Circuits from Information Stored in Simulation Dump Files
US	Published	12/332291	12/10/2008			Coherent Instruction Cache Utilizing Cache-Op Execution Resources
US	Published	12/357929	1/22/2009			Processor Accessing a Scratch Pad On-Demand to Reduce Power Consumption
US	Published	12/399330	3/6/2009			Configurable Instruction Sequence Generation
US	Published	12/409363	3/23/2009			Round-Robin Apparatus and Instruction Dispatch Scheduler Employing Same For Use In Multithreading Microprocessor
US	Published	12/411913	3/26/2009			Method and Apparatus for Improved Computer Load and Store Operations

US	Published	12/429029	4/23/2009	Apparatus for Storing Instructions In a Multithreading Microprocessor
US	Published	12/429655	4/24/2009	Data Transfer Bus Communication Using Single Request to Perform Command and Return Data to Context Associated Destination Registration (Amended)
US	Published	12/463330	5/8/2009	Microprocessor with Compact Instruction Set Architecture
US	Published	12/464027	5/11/2009	Variable Register and Immediate Field Encoding in an Instruction Set Architecture
US	Published	12/563840	9/21/2009	Data Cache Virtual Hint Way Prediction, and Applications Thereof {as amended from} Data Cache Virtual Hint Based Way Prediction
US	Published	12/652598	1/5/2010	System and Method for Improving Memory Transfer {amended from: String Copy Instruction and System to Implement the Same}

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Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
US	Published	12/748102	3/26/2010			Microprocessor with Compact Instruction Set Architecture
US	Published	12/794370	6/4/2010			Processor Core and Method for Managing Program Counter Redirection in an Out-of-Order Processor Pipeline
US	Published	12/828056	6/30/2010			Horizontally-Shared Cache Victims in Multiple Core Processors
US	Published	12/847772	7/30/2010			Hardware Interrupt Handling
US	Published	12/875268	9/3/2010			Alignment and Ordering of Vector Elements for Single Instruction Multiple Data Processing
US	Published	12/891530	9/27/2010			MICROPROCESSOR SYSTEM FOR VIRTUAL MACHINE EXECUTION
US	Published	12/911901	10/26/2010			Symmetric Multiprocessor Operating System for Execution on Non-Independent Lightweight Thread Contexts
US	Published	13/027917	2/15/2011			Automated Digital Circuit Design Tool that Reduces or Eliminates Adverse Timing Constraints Due to an Inherent Clock Signal Skew, and Applications Thereof
US	Published	13/034567	2/24/2011			Apparatus and Method for Controlling the Exclusivity Mode of a Level-Two Cache
US	Published	13/041948	3/7/2011			Interrupt and Exception Handling for Multi-Streaming Digital Processors
US	Published	13/277856	10/20/2011			Clock Ratio Controller for Dynamic Voltage and Frequency Scaled Digital Systems, and Applications Thereof
US	Published	13/323006	12/12/2011			Method and Apparatus for Predicting Characteristics of Incoming Data Packets to Enable Speculative Processing to Reduce Processor Latency

Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
KR	Granted	89-1826	2/17/1989	192138	1/28/1999	Variable Delay Line Phase-Locked Loop Circuit
DE	Granted	4312250.7	4/15/1993	4312250	8/25/2005	System and Method for Booting Computer for Operation in Either of Two Byte-Order Modes
JP	Granted	5-152820	5/31/1993	3186905	5/11/2001	System and Method for Booting Computer for Operation in Either of Two Byte-Order Modes
FR	Granted	94915938.8	4/28/1994	0699318	12/5/2001	Unified Floating Point and Integer Datapath for a RISC Processor
GB	Granted	94915938.8	4/28/1994	0699318	12/5/2001	Unified Floating Point and Integer Datapath for a RISC Processor
DE	Granted	94915938.8	4/28/1994	69429342.3	12/5/2001	Unified Floating Point and Integer Datapath for a RISC Processor
EP	Granted	94915938.8	4/28/1994	0699318	12/5/2001	Unified Floating Point and Integer Datapath for a RISC Processor
FR	Granted	95904903.2	12/12/1994	0734553	3/19/2003	Apparatus for Processing Instructions in a Computing System
GB	Granted	95904903.2	12/12/1994	0734553	3/19/2003	Apparatus for Processing Instructions in a Computing System
DE	Granted	95904903.2	12/12/1994	69432314.4	3/19/2003	Apparatus for Processing Instructions in a Computing System
EP	Granted	95904903.2	12/12/1994	0734553	3/19/2003	Apparatus for Processing Instructions in a Computing System
GB	Granted	95902961.2	12/15/1994	0690372	3/3/2010	Superscalar Microprocessor Instruction Pipeline Including Dispatching and Kill Control
EP	Granted	95902961.2	12/15/1994	0690372	3/3/2010	Superscalar Microprocessor Instruction Pipeline Including Dispatching and Kill Control
TW	Granted	84101225	2/11/1995	101058	6/14/1999	Superscalar Microprocessor Instruction Pipeline Including Dispatching and Kill Control
SG	Granted	9604602-4	12/15/1994	75774	11/22/2001	Superscalar Microprocessor Instruction Pipeline Including Dispatching and Kill Control

CN	Granted	94191501.8	12/15/1994	94191501.8	7/11/2001	Superscalar Microprocessor Instruction Pipeline Including Dispatching and Kill Control
FR	Granted	95902961.2	12/15/1994	0690372	3/3/2010	Superscalar Microprocessor Instruction Pipeline Including Dispatching and Kill Control
KR	Granted	95-703431	12/15/1994	175116	11/7/1998	Superscalar Microprocessor Instruction Pipeline Including Dispatching and Kill Control
JP	Granted	7-516665	12/15/1994	2815236	8/14/1998	Superscalar Microprocessor Instruction Pipeline Including Dispatching and Kill Control

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Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
DE	Granted	95902961.2	12/15/1994	0690372	3/3/2010	Superscalar Microprocessor Instruction Pipeline Including Dispatching and Kill Control
EP	Granted	95902965.3	12/15/1994	0690373	3/17/2004	Apparatus for Processing Instructions in a Computing System
KR	Granted	95-703432	12/15/1994	212204	5/8/1999	Apparatus for Processing Instructions in a Computing System
TW	Granted	84101274	2/13/1995	078360	9/18/1996	Apparatus for Processing Instructions in a Computing System
JP	Granted	7-516669	12/15/1994	2815237	8/14/1998	Apparatus for Processing Instructions in a Computing System
DE	Granted	95902965.3	12/15/1994	69433621.1	3/17/2004	Apparatus for Processing Instructions in a Computing System
GB	Granted	95902965.3	12/15/1994	0690373	3/17/2004	Apparatus for Processing Instructions in a Computing System
CN	Granted	94191180.2	12/15/1994	94191180.2	4/2/2003	Apparatus for Processing Instructions in a Computing System
FR	Granted	95902965.3	12/15/1994	0690373	3/17/2004	Apparatus for Processing Instructions in a Computing System
CN	Granted	02140762.2	12/15/1994	02140762.2	8/2/2006	Apparatus for Processing Instructions in a Computing System
HK	Granted	98114553.3	12/22/1998	1018168	9/6/2002	Mechanism and Method for Integer Divide Involving Pre-Alignment of the Divisor Relative to the Dividend
TW	Granted	84101214	2/11/1995	079922	11/29/1996	Mechanism and Method for Integer Divide Involving Pre-Alignment of the Divisor Relative to the Dividend
CN	Granted	94191178.0	12/15/1994	94191178.0	3/12/2003	Mechanism and Method for Integer Divide Involving Pre-Alignment of the Divisor Relative to the Dividend
KR	Granted	95-703430	12/15/1994	305544	7/31/2001	Mechanism and Method for Integer Divide Involving Pre-Alignment of the Divisor Relative to the Dividend
EP	Granted	95902962.0	12/15/1994	0684548	3/6/2002	Mechanism and Method for Integer Divide Involving Pre-Alignment of the Divisor Relative to the Dividend
GB	Granted	95902962.0	12/15/1994	0684548	3/6/2002	Mechanism and Method for Integer Divide Involving Pre-Alignment of the Divisor Relative to the Dividend
DE	Granted	95902962.0	12/15/1994	69430053	3/6/2002	Mechanism and Method for Integer Divide Involving Pre-Alignment of the Divisor Relative to the Dividend
FR	Granted	95902962.0	12/15/1994	0684548	3/6/2002	Mechanism and Method for Integer Divide Involving Pre-Alignment of the Divisor Relative to the Dividend
DE	Granted	95902964.6	12/15/1994	69434728.0-08	5/10/2006	System and Method for Coherency in a Split-Level Data Cache System
KR	Granted	95-703429	12/15/1994	182344	12/11/1998	System and Method for Coherency in a Split-Level Data Cache System
FR	Granted	95902964.6	12/15/1994	0684561	5/10/2006	System and Method for Coherency in a Split-Level Data Cache System
TW	Granted	84101223	2/11/1995	106608	1/7/2000	System and Method for Coherency in a Split-Level Data Cache System
EP	Granted	95902964.6	12/15/1994	0684561	5/10/2006	System and Method for Coherency in a Split-Level Data Cache System
CN	Granted	94191177.2	12/15/1994	94191177.2	2/26/2000	System and Method for Coherency in a Split-Level Data Cache System
SG	Granted	9604743-6	12/15/1994	75776	2/20/2001	System and Method for Coherency in a Split-Level Data Cache System
GB	Granted	95902964.6	12/15/1994	0684561	5/10/2006	System and Method for Coherency in a Split-Level Data Cache System

HK	Granted	98114540.9	12/15/1994	1018166	9/22/2006	System and Method for Coherency in a Split-Level Data Cache System
JP	Granted	07-516668	12/15/1994	2631037	4/25/1997	System and Method for Coherency in a Split-Level Data Cache System
DE	Granted	95902963.8	12/15/1994	69428110.7	8/29/2001	Debug Mode for a Superscalar RISC Processor
EP	Granted	95902963.8	12/15/1994	0684552	8/29/2001	Debug Mode for a Superscalar RISC Processor
CN	Granted	94191179.9	12/15/1994	94191179.9	5/8/2002	Debug Mode for a Superscalar RISC Processor
FR	Granted	95902963.8	12/15/1994	0684552	8/29/2001	Debug Mode for a Superscalar RISC Processor
GB	Granted	95902963.8	12/15/1994	0684552	8/29/2001	Debug Mode for a Superscalar RISC Processor
HK	Granted	98114541.8	12/15/1994	1018167	1/18/2002	Debug Mode for a Superscalar RISC Processor
TW	Granted	84101222	2/11/1995	078040	8/29/1996	Debug Mode for a Superscalar RISC Processor

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Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
JP	Granted	7-516667	12/15/1994	2843152	10/23/1998	Debug Mode for a Superscalar RISC Processor
KR	Granted	95-703428	12/15/1994	175115	11/7/1998	Debug Mode for a Superscalar RISC Processor
SG	Granted	2000012542	9/18/1998	71539	5/29/2002	Instruction Prediction Based on Filtering
JP	Granted	2001-514658	7/24/2000	4691294	2/25/2011	Processor with Improved Accuracy for Multiply-Add Operations
FR	Granted	02717430.9	2/15/2002	1374034	4/23/2008	Extended Precision Accumulator
DE	Granted	02717430.9	2/15/2002	1374034	4/23/2008	Extended Precision Accumulator
EP	Granted	02717430.9	2/15/2002	1374034	4/23/2008	Extended Precision Accumulator
GB	Granted	02717430.9	2/15/2002	1374034	4/23/2008	Extended Precision Accumulator
CN	Granted	02808541.8	2/15/2002	02808541.8	10/1/2008	Polynomial Arithmetic Operations
FR	Granted	02707785.8	2/15/2002	1379939	9/21/2011	Partial Bitwise Permutations
GB	Granted	02707785.8	2/15/2002	1379939	9/21/2011	Partial Bitwise Permutations
EP	Granted	02707785.8	2/15/2002	1379939	9/21/2011	Partial Bitwise Permutations
DE	Granted	02707785.8	2/15/2002	1379939	9/21/2011	Partial Bitwise Permutations
JP	Granted	2002-568190	2/15/2002	3837113	8/4/2006	Partial Bitwise Permutations
CN	Granted	02808631.7	2/15/2002	02808631.7	11/26/2008	Partial Bitwise Permutations
EP	Granted	02749511.8	3/8/2002	1410218	8/27/2008	Mechanism for Programmable Modification of Memory Mapping Granularity
GB	Granted	02749511.8	3/8/2002	1410218	8/27/2008	Mechanism for Programmable Modification of Memory Mapping Granularity
DE	Granted	60228580.0	3/8/2002	1410208	8/27/2008	Mechanism for Programmable Modification of Memory Mapping Granularity
FR	Granted	02749511.8	3/8/2002	1410218	8/27/2008	Mechanism for Programmable Modification of Memory Mapping Granularity
JP	Granted	2002-578154	3/8/2002	4256167	3/8/2002	Mechanism to Extend Computer Memory Protection Schemes
CN	Granted	03821190.4	8/25/2003	03821190.4	5/8/2009	Method and Apparatus for Clearing Hazards Using Jump Instructions
IN	Granted	482/DELNP/2005	8/25/2003	249550	10/25/2011	Method and Apparatus for Clearing Hazards Using Jump Instructions
JP	Granted	2004-534327	8/25/2003	4030999	10/26/2007	Method and Apparatus for Clearing Hazards Using Jump Instructions
FR	Granted	02804389.1	9/10/2002	1442375	12/27/2006	Method and Apparatus for Binding Shadow Registers to Vectored Interrupts
GB	Granted	02804389.1	9/10/2002	1442375	12/27/2006	Method and Apparatus for Binding Shadow Registers to Vectored Interrupts
HK	Granted	05100480.2	9/10/2002	1070147	7/20/2007	Method and Apparatus for Binding Shadow Registers to Vectored Interrupts
DE	Granted	02804389.1	9/10/2002	60217157.1	12/27/2006	Method and Apparatus for Binding Shadow Registers to Vectored Interrupts
EP	Granted	02804389.1	9/10/2002	1442375	12/27/2006	Method and Apparatus for Binding Shadow Registers to Vectored Interrupts
EP	Granted	03721791.6	4/17/2003	1499978	3/11/2009	Mechanism for Reduction of Operations Between Interfaces
GB	Granted	03721791.6	4/17/2003	1499978	3/11/2009	Mechanism for Reduction of Operations Between Interfaces
FR	Granted	03721791.6	4/17/2003	1499978	3/11/2009	Mechanism for Reduction of Operations Between Interfaces
HK	Granted	05105771.9	4/17/2003	HK1078352	4/17/2003	Mechanism for Reduction of Operations Between Interfaces
DE	Granted	03721791.6	4/17/2003	1499978	3/11/2009	Mechanism for Reduction of Operations Between Interfaces
JP	Granted	2000-588668	12/13/1999	3877527	11/10/2006	Prioritized Instruction Scheduling for Multi-Streaming Processors
JP	Granted	2000-596449	12/13/1999	3880034	11/17/2006	Register Transfer Unit for Electronic Processor

JP	Granted	2000-607105	3/14/2000	3877529	11/10/2006	Interstream Control and Communications for Multi-Streaming Digital Processors
JP	Granted	2001-554162	1/3/2001	3721129	9/16/2005	Method and Apparatus for Improved Computer Load and Store Operations
FR	Granted	01900915.8	1/3/2001	1257912	8/19/2009	Method and Apparatus for Improved Computer Load and Store Operations
GB	Granted	01900915.8	1/3/2001	1257912	8/19/2009	Method and Apparatus for Improved Computer Load and Store Operations
DE	Granted	01900915.8	1/3/2001	1257912	8/19/2009	Method and Apparatus for Improved Computer Load and Store Operations

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Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
EP	Granted	01900915.8	1/3/2001	1257912	8/19/2009	Method and Apparatus for Improved Computer Load and Store Operations
DE	Granted	01901882.9	1/8/2001	1259888	3/3/2010	Queuing System for Processors in Packet Routing Operations
JP	Granted	2001-558844	1/8/2001	3801919	5/12/2006	Queuing System for Processors in Packet Routing Operations
GB	Granted	01901882.9	1/8/2001	125988	3/3/2010	Queuing System for Processors in Packet Routing Operations
FR	Granted	01901882.9	1/8/2001	125988	3/3/2010	Queuing System for Processors in Packet Routing Operations
EP	Granted	01901882.9	1/8/2001	125988	3/3/2010	Queuing System for Processors in Packet Routing Operations
GB	Granted	01952463.6	7/5/2001	1311947	1/19/2011	Instruction Fetch and Dispatch in Multithreaded System
FR	Granted	01952463.6	7/5/2001	1311947	1/19/2011	Instruction Fetch and Dispatch in Multithreaded System
DE	Granted	01952463.6	7/5/2001	1311947	1/19/2011	Instruction Fetch and Dispatch in Multithreaded System
EP	Granted	01952463.6	7/5/2001	1311947	1/19/2011	Instruction Fetch and Dispatch in Multithreaded System
JP	Granted	2002-511080	6/7/2001	4926364	2/17/2012	Method and Apparatus for Implementing Atomicity of Memory Operations in Dynamic Multi-Streaming Processors
EP	Granted	01944671.5	6/7/2001	1299801	12/29/2010	Implementing Atomicity of Memory Operations (as amended from: Method and Apparatus for Implementing Atomicity of Memory Operations in Dynamic Multi-Streaming Processors)
FR	Granted	01944671.5	6/7/2001	1299801	12/29/2010	Implementing Atomicity of Memory Operations (as amended from: Method and Apparatus for Implementing Atomicity of Memory Operations in Dynamic Multi-Streaming Processors)
DE	Granted	01944671.5	6/7/2001	1299801	12/29/2010	Implementing Atomicity of Memory Operations (as amended from: Method and Apparatus for Implementing Atomicity of Memory Operations in Dynamic Multi-Streaming Processors)
GB	Granted	01944671.5	6/7/2001	1299801	12/29/2010	Implementing Atomicity of Memory Operations (as amended from: Method and Apparatus for Implementing Atomicity of Memory Operations in Dynamic Multi-Streaming Processors)
FR	Granted	04786607.4	8/27/2004	1660993	11/19/2008	Integrated Mechanism for Suspension and Deallocation of Computational Threads of Execution in a Processor
EP	Granted	04786607.4	8/27/2004	1660993	11/19/2008	Integrated Mechanism for Suspension and Deallocation of Computational Threads of Execution in a Processor
CN	Granted	200480024852.9	8/27/2004	714533	8/9/2010	Method and Apparatus for Performing Parallel Program Threads {amended from} Integrated Mechanism for Suspension and Deallocation of Computational Threads of Execution in a Processor
IN	Granted	1341/DELNP/2006	8/26/2004	244906	12/24/2010	Integrated Mechanism for Suspension and Deallocation of Computational Threads of Execution in a Processor
GB	Granted	04786607.4	8/27/2004	1660993	11/19/2008	Integrated Mechanism for Suspension and Deallocation of Computational Threads of Execution in a Processor
DE	Granted	04786607.4	8/27/2004	1660993	11/19/2008	Integrated Mechanism for Suspension and Deallocation of Computational Threads of Execution in a Processor
JP	Granted	2006/524929	8/27/2004	4818919	9/9/2011	Integrated Mechanism for Suspension and Deallocation of Computational Threads of Execution in a Processor
IN	Granted	1303/DELNP/2006	8/27/2004	248427	7/13/2011	Integrated Mechanism for Suspension and Deallocation of Computational Threads of Execution in a Processor

CN	Granted	200510067702.2	4/22/2005	200510067702.2	9/23/2009	Method and Apparatus for Recoding Instructions
JP	Granted	2006/524868	8/27/2004	4818918	9/9/2011	Instruction for Initiation of Concurrent Instruction Streams in a Multithreading Microprocessor {f.k.a.} Improved Mechanism for Initiation of Concurrent Instruction Streams in a Multithreading Multiprocessor
CN	Granted	200480024798.8	8/27/2004	200480024798.8	1/23/2009	Multithreaded Microprocessor, Method for Creating New Thread and Multithreaded Processing System (as amended)
JP	Granted	2006/524900	8/27/2004	4740851	5/13/2011	Mechanisms for Dynamic Configuration of Virtual Processor Resources
CN	Granted	200480024801.6	8/27/2004	546615	5/8/2009	Mechanisms for Dynamic Configuration of Virtual Processor Resources
TW	Granted	094127943	8/16/2005	I294588	3/11/2008	Microprocessor Instruction Using Address Index Values to Enable Access of a Virtual Buffer in Circular Fashion

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Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
EP	Granted	05789110.3	8/11/2005	1709526	12/17/2008	Processor, Method and Computer Program Products for Execution of Instructions for Efficient Bit Stream Extractions
HK	Granted	07102289.9	2/28/2007	1097928	4/9/2009	Microprocessor Instructions for Efficient Bit Stream Extractions
FR	Granted	05789110.3	8/11/2005	1709526	12/17/2008	Processor, Method and Computer Program Products for Execution of Instructions for Efficient Bit Stream Extractions
DE	Granted	602005011756.3	8/11/2005	1709526	12/17/2008	Processor, Method and Computer Program Products for Execution of Instructions for Efficient Bit Stream Extractions
GB	Granted	05789110.3	8/11/2005	1709526	12/17/2008	Processor, Method and Computer Program Products for Execution of Instructions for Efficient Bit Stream Extractions
TW	Granted	095102946	1/25/2006	I316203	10/21/2009	Bifurcated Instruction Dispatch Scheduler in a Multi-Threading Microprocessor
CN	Granted	200680003641.6	1/18/2006	559626	1/18/2010	Multithreading Mircoprocessor with Optimized Thread Scheduler for Increasing Pipeline Utilization Efficiency
GB	Granted	0714145.0	1/18/2006	2436501	7/29/2009	Multithreading Mircoprocessor with Optimized Thread Scheduler
GB	Granted	0719536.5	3/28/2006	2439253	11/12/2008	Apparatus and Method for Software Specified Power Management Performance Using Low Power Virtual Threads
CN	Granted	200680016775.1	3/28/2006	ZL200680016775.1	11/16/2011	Apparatus and Method for Software Specified Power Management Performance Using Low Power Virtual Threads
KR	Granted	10-2007-702639	11/13/2007	10-1100470	12/22/2011	Apparatus and Method for Automatic Low Power Mode Invocation in a Multi-Threaded Processor
CN	Granted	200680050617.8	11/15/2006	ZL200680050617.8	1/25/2012	Microprocessor Having a Power-Saving Instruction Cache Way Predictor and Instruction Replacement Scheme {amended from: A Cache Way Predictor Scheme}
GB	Granted	0814234.1	2/12/2007	2448276	6/15/2011	Distributive Scoreboard Scheduling in an Out-of-Order Processor f.k.a. {A Counter Approach for Distributive Scoreboard Scheduling in an Out-of-Order Microprocessor}
CN	Granted	200780036981.3	8/15/2007	ZL200780036981.3	6/22/2011	Micro Tag Reducing Cache Power
GB	Granted	0903127.9	8/15/2007	2456636	10/26/2011	Processor Having a Micro Tag Array that Reduces Data Cache Access Power, and Applications Thereof_{amended from_ Micro Tag Array to Preserve Data Cache Access Power_}
CN	Granted	200780042526.4	9/28/2007	ZL200780042526.4	12/28/2011	Data Cache Virtual Hint Way Prediction, and Applications Thereof {f.k.a.}__ Data Cache Virtual Hint Based Way Prediction
GB	Granted	0904890.1	9/28/2007	2455457	8/3/2011	Data Cache Virtual Hint Based Way Prediction
CN	Granted	200780043374.X	9/28/2007	100037	10/28/2011	Load/Store Unit for a Processor, and Applications Thereof
GB	Granted	0904889.3	9/28/2007	2455254	8/10/2011	Twice Issued Conditional Move Instruction, and Applications Thereof (as amended)

						Twice Issued Integer Condition Move
GB	Granted	0922079.9	6/20/2008	2463409	11/2/2011	Preventing Writeback Race in Multiple Core Processors {f.k.a.} Mechanism for Solving a Writeback Race in CMP Systems
WO	NAT PHASE	US87/03422	12/23/1987			RISC Computer with Unaligned Reference Handling and Method for the Same
WO	NAT PHASE	US94/04701	4/28/1994			Unified Floating Point and Integer Datapath for a RISC Processor
WO	NAT PHASE	US94/14380	12/12/1994			Apparatus for Processing Instructions in a Computing System
WO	NAT PHASE	JP94/02108	12/15/1994			Superscalar Microprocessor Instruction Pipeline Including Dispatching and Kill Control
WO	NAT PHASE	JP94/02112	12/15/1994			Apparatus for Processing Instructions in a Computing System
WO	NAT PHASE	JP94/02109	12/15/1994			Mechanism and Method for Integer Divide Involving Pre-Alignment of the Divisor Relative to the Dividend
WO	NAT PHASE	JP94/02111	12/15/1994			System and Method for Coherency in a Split-Level Data Cache System
WO	NAT PHASE	JP94/02110	12/15/1994			Debug Mode for a Superscalar RISC Processor

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
WO	NAT PHASE	US95/13241	10/13/1995			Indexing & Multiplexing of Interleaved Cache Memory Arrays
WO	NAT PHASE	US98/19674	9/18/1998			Instruction Prediction Based on Filtering
WO	NAT PHASE	US00/03900	2/14/2000			Processor Having a Compare Extension of an Instruction Set Architecture
WO	NAT PHASE	US00/20160	7/24/2000			Processor with Improved Accuracy for Multiply-Add Operations
WO	NAT PHASE	2002/04414	2/15/2002			Extended Precision Accumulator
WO	NAT PHASE	2002/04415	2/15/2002			Polynomial Arithmetic Operations
WO	NAT PHASE	2002/04427	2/15/2002			Partial Bitwise Permutations
WO	NAT PHASE	2002/07205	3/8/2002			Mechanism for Programmable Modification of Memory Mapping Granularity
WO	NAT PHASE	2002/07206	3/8/2002			Mechanism to Extend Computer Memory Protection Schemes
WO	NAT PHASE	2003/26600	8/25/2003			Method and Apparatus for Clearing Hazards Using Jump Instructions
WO	NAT PHASE	2002/28893	9/10/2002			Method and Apparatus for Binding Shadow Registers to Vectored Interrupts
WO	NAT PHASE	2003/12200	4/17/2003			Mechanism for Reduction of Operations Between Interfaces
WO	NAT PHASE	US99/29645	12/13/1999			Prioritized Instruction Scheduling for Multi-Streaming Processors
WO	NAT PHASE	US99/29646	12/13/1999			Register Transfer Unit for Electronic Processor
WO	NAT PHASE	US00/06615	3/14/2000			Interstream Control and Communications for Multi-Streaming Digital Processors
WO	NAT PHASE	US01/00413	1/3/2001			Method and Apparatus for Improved Computer Load and Store Operations
WO	NAT PHASE	US01/00587	1/8/2001			Queuing System for Processors in Packet Routing Operations
WO	NAT PHASE	US01/21372	7/5/2001			Methods and Apparatus for Improving Fetching and Dispatch of Instructions in Multithreaded Processor
WO	NAT PHASE	US01/40900	6/7/2001			Method and Apparatus for Implementing Atomicity of Memory Operations in Dynamic Multi-Streaming Processors
WO	NAT PHASE	2004/029272	8/26/2004			Integrated Mechanism for Suspension and Deallocation of Computational Threads of Execution in a Processor
WO	NAT PHASE	2004/028108	8/27/2004			Integrated Mechanism for Suspension and Deallocation of Computational Threads of Execution in a Processor
WO	NAT PHASE	2004/027827	8/27/2004			Improved Mechanism for Initiation of Concurrent Instruction Streams
WO	NAT PHASE	2004/027976	8/27/2004			Mechanisms for Dynamic Configuration of Virtual Processor Resources
WO	NAT PHASE	2005/028773	8/11/2005			Microprocessor Instruction Using Address Index Values to Enable Access of a Virtual Buffer in Circular Fashion
WO	NAT PHASE	2005/028774	8/11/2005			Microprocessor Instructions for Efficient Bit Stream Extractions
WO	NAT PHASE	2006/001557	1/18/2006			Bifurcated Thread Scheduler in a Multithreading Microprocessor

WO	NAT PHASE	2006/001558	1/18/2006			Multithreading Mircoprocessor with Optimized Thread Scheduler for Increasing Pipeline Utilization Efficiency
WO	NAT PHASE	2006/011326	3/28/2006			Apparatus and Method for Software Specified Power Management Performance Using Low Power Virtual Threads
WO	NAT PHASE	2006/011327	3/28/2006			Apparatus and Method for Automatic Low Power Mode Invocation in a Multi-Threaded Processor
WO	NAT PHASE	2009/002893	5/8/2009			Microprocessor with Compact Instruction Set Architecture

Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
EP	Allowed	06739851.1	3/28/2006			MULTI-THREADED PROCESSOR COMPRISING CUSTOMIZABLE BIFURCATED THREAD SCHEDULER FOR AUTOMATIC LOW POWER MODE INVOCATION
HK	Pending	98114200.0	12/21/1998			Superscalar Microprocessor Instruction Pipeline Including Dispatching and Kill Control

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
HK	Pending	98114187.7	12/21/1998			Apparatus for Processing Instructions in a Computing System
JP	Pending	07-516666	12/15/1994			Mechanism and Method for Integer Divide Involving Pre-Alignment of the Divisor Relative to the Dividend
JP	Pending	2002-512805	7/5/2001			Methods and Apparatus for Improving Fetching and Dispatch of Instructions in Multithreaded Processor
IN	Pending	1339/DELNP/2006	8/27/2004			Apparatus, Method, and Instruction for Initiation of Concurrent Instruction Streams in a Multithreading Microprocessor {f.k.a.}__Improved Mechanism for Initiation of Concurrent Instruction Streams
IN	Pending	1340/DELNP/2006	8/27/2004			Mechanisms for Dynamic Configuration of Virtual Processor Resources
IN	Pending	5816/DELNP/2007	1/18/2006			Bifurcated Thread Scheduler in a Multithreading Microprocessor
KR	Pending	07-7018690	1/18/2006			Bifurcated Thread Scheduler in a Multithreading Microprocessor
IN	Pending	5815/DELNP/2007	1/18/2006			Multithreading Mircoprocessor with Optimized Thread Scheduler for Increasing Pipeline Utilization Efficiency
JP	Pending	2008-506488	3/28/2006			Apparatus and Method for Automatic Low Power Mode Invocation in a Multi-Threaded Processor
IN	Pending	8449/DELNP/2007	3/28/2006			Apparatus and Method for Automatic Low Power Mode Invocation in a Multi-Threaded Processor
TW	Pending	95140051	10/30/2006			Two Step Kill Mechanism Upon Branch Mispredict Resolution in OOO Pipeline
IN	Pending	1983/KOLNP/2008	11/15/2006			Loop Buffer for Fetch Power Saving in MIPS Cores
IN	Pending	1982/KOLNP/2008	11/15/2006			A Cache Way Predictor Scheme
IN	Pending	3596/KOLNP/2008	2/12/2007			A Counter Approach for Distributive Scoreboard Scheduling in an Out-of-Order Microprocessor
IN	Pending	596/KOLNP/2009	8/15/2007			Micro Tag Array to Preserve Data Cache Access Power
IN	Pending	1084/KOLNP/2009	3/20/2009			Apparatus and Method for Tracing Instructions with Simplified Instruction State Descriptors
IN	Pending	1089/KOLNP/2009	9/28/2007			Data Cache Virtual Hint Based Way Prediction
IN	Pending	1276/KOLNP/2009	9/28/2007			Twice Issued Conditional Move Instruction and Applications Thereof
WO	Pending	2007/088351	12/20/2007			Efficient Resource Arbitration
WO	Pending	2008/000220	2/1/2008			Software and Techniques for Generation of Self-Checking Random Programs
WO	Pending	2008/67676	6/20/2008			Mechanism for Solving a Writeback Race in CMP Systems
WO	Pending	2008/067705	6/20/2008			Method for Reducing Handling of Write Data
WO	Pending	2008/067719	6/20/2008			Methods for Avoiding Livelock in Multi-Core Systems
IN	Pending	224/KOLNP/2010	8/29/2008			Low-Overhead/Power-Saving Processor Synchronization Mechanism, and Applications Thereof
CN	Pending	200880104604.3	8/29/2008			Low-Overhead/Power-Saving Processor Synchronization Mechanism, and Applications Thereof
WO	Pending	2008/010234	8/29/2008			Low-Overhead/Power-Saving Processor Synchronization Mechanism, and Applications Thereof
IN	Pending	4217/KOLNP/2010	5/8/2009			Microprocessor with Compact Instruction Set Architecture

CN	Pending	201110128200.1	3/25/2011	Microprocessor with Compact Instruction Set Architecture
HK	Pending	11112712.9	3/25/2011	Microprocessor with Compact Instruction Set Architecture
HK	Pending	11112196.4	5/8/2009	Microprocessor with Compact Instruction Set Architecture
IN	Pending	2359/KOLNP/2011	1/21/2010	System and Method for Improving Memory Transfer
WO	Pending	2010/21620	1/21/2010	String Copy Instruction and System to Implement the Same
CN	Pending	201010178234.7	5/11/2010	Variable Register and Immediate Field Encoding in an Instruction Set Architecture
IN	Pending	911/KOL/2011	7/6/2011	System and Method for Automatic Hardware Interrupt Handling
EP	Published	03003266.8	12/15/1994	Apparatus for Processing Instructions in a Computing System
EP	Published	00919300.4	2/14/2000	Processor Having a Compare Extension of an Instruction Set Architecture
JP	Published	2009-131836	6/1/2009	Extended Precision Accumulator
CN	Published	02808633.3	2/15/2002	Extended Precision Accumulator
EP	Published	02717593.4	3/8/2002	Mechanism to Extend Computer Memory Protection Schemes

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

Ctry	Status	AppNum	FilDate	PatNum	IssDate	AppTitle
HK	Published	05110923.6	11/30/2005			Method and Apparatus for Clearing Hazards Using Jump Instructions
EP	Published	03751894.1	8/25/2003			Method and Apparatus for Clearing Hazards Using Jump Instructions
HK	Published	07107764.2	7/18/2007			Method and Apparatus for Binding Shadow Registers to Vectored Interrupts
EP	Published	04783500.4	8/26/2004			Suspension and Deallocation of Computational Threads of Execution in a Processor
CN	Published	200480024800.1	8/26/2004			Integrated Mechanism for Suspension and Deallocation of Computational Threads of Execution in a Processor
EP	Published	04782325.7	8/27/2004			Initiation of Concurrent Instructions Streams {f.k.a.} Improved Mechanism for Initiation of Concurrent Instruction Streams
EP	Published	04782455.2	8/27/2004			Mechanisms for Dynamic Configuration of Virtual Processor Resources
HK	Published	07102292.4	2/28/2007			Microprocessor Instruction to Enable Access of a Virtual BUffer in Circular Fashion
EP	Published	06718610.6	1/18/2006			Bifurcated Thread Scheduler in a Multithreading Microprocessor
CN	Published	200680003639.9	1/18/2006			Bifurcated Thread Scheduler in a Multithreading Microprocessor
IN	Published	8450/DELNP/2007	3/28/2006			Apparatus and Method for Software Specified Power Management Performance Using Low Power Virtual Threads
CN	Published	200680016774.7	3/28/2006			Apparatus and Method for Automatic Low Power Mode Invocation in a Multi-Threaded Processor
WO	Published	2006/044354	11/15/2006			Processor Utilizing a Loop Buffer to Reduce Power Consumption
CN	Published	200680050607.4	11/15/2006			Processor Utilizing A Loop Buffer to Reduce Power Consumption
WO	Published	2006/044355	11/15/2006			Microprocessor Having a Power-Saving Instruction Cache Way Predictor and Instruction Replacement Scheme
WO	Published	2007/003752	2/12/2007			Distributive Scoreboard Scheduling in an Out-of-Order Microprocessor
CN	Published	200780007020.X	2/12/2007			A Counter Approach for Distributive Scoreboard Scheduling in an Out-of-Order Microprocessor
WO	Published	2007/017896	8/15/2007			Micro Tag Array to Preserve Data Cache Access Power
WO	Published	2007/078617	9/17/2007			Apparatus and Method for Tracing Instructions with Simplified Instruction State Descriptors
CN	Published	200780035943.6	3/27/2009			Apparatus and Method for Tracing Instructions with Simplified Instruction State Descriptors
WO	Published	2007/021007	9/28/2007			Data Cache Virtual Hint Based Way Prediction, and Applications Thereof
WO	Published	2007/021006	9/28/2007			Load/Store Unit for a Processor, and Applications Thereof
WO	Published	2007/021005	9/28/2007			Twice Issued Conditional Move Instruction, and Applications Thereof
CN	Published	200780041776.6	9/28/2007			Twice Issued Integer Condition Move
WO	Published	2007/087632	12/14/2007			Speculative Cache Tag Evaluation
TW	Published	97103841	2/1/2008			A SYSTEM, METHOD AND SOFTWARE APPLICATION FOR THE GENERATION OF VERIFICATION PROGRAMS
CN	Published	200880103410.1	6/20/2008			Mechanism for Solving a Writeback Race in CMP Systems

CN	Published	200880103458.2	6/20/2008	Methods for Avoiding Livelock in Multi-Core Systems
GB	Published	1002970.0	8/29/2008	Low-Overhead/Power-Saving Processor Synchronization Mechanism, and Applications Thereof
CN	Published	200880108013.3	9/19/2008	Support for Multiple Coherence Domains
WO	Published	2008/077084	9/19/2008	Support for Multiple Coherence Domains
CN	Published	200980124104.0	5/8/2009	Microprocessor with Compact Instruction Set Architecture
CN	Published	201080005211.4	1/21/2010	System and Method for Improving Memory Transfer {f.k.a.} String Copy Instruction and System to Implement the Same
CN	Published	201110214684.1	7/29/2011	System and Method for Automatic Hardware Interrupt Handling

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

Exhibit B:
Disclosure Schedule

[*].

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

Exhibit C:
Affiliates of MIPS Technologies, Inc. as of June 29, 2012

1. MIPS Technologies International Ltd. (Cayman Islands)
2. MIPS Technologies (Shanghai) Co., Ltd.
3. MIPS Technologies B.V (Netherlands), including the following branch offices:
   (i) MIPS Technologies BV (Netherlands), Japan Branch
   (ii) MIPS Technologies BV (Netherlands), Germany Branch
   (iii) MIPS Technologies BV (Netherlands), Israel Branch
   (iv) MIPS Technologies BV (Netherlands), Taiwan Branch
   (v) MIPS Technologies BV (Netherlands), Korea Branch

State qualifications in California, Colorado, Florida, New Jersey, New York, Florida and Washington

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

Attachment 1
AMENDMENT 6 TO
2007 MIPS CORES LICENSE AGREEMENT

This Amendment No. 6 to 2007 MIPS Cores License Agreement ("Amendment 6") is made effective as of June 29, 2012 (the "Amendment 6 Effective Date") by and between Broadcom Corporation, a Delaware corporation with its principal place of business at 5300 California Avenue, Irvine, California 92617 ("Broadcom") and MIPS Technologies, Inc., a Delaware corporation with its principal place of business at 955 East Arques Ave., Sunnyvale, California 94085 ("MIPS"). Unless otherwise indicated below, any capitalized terms in this Amendment 6 not defined herein shall have the applicable meaning set forth in the 2007 MIPS Cores License Agreement between MIPS and Broadcom dated January 26, 2007, as amended (the "2007 License Agreement").

WHEREAS, the parties desire to amend and extend certain terms of the 2007 License Agreement, as set forth herein;

NOW, THEREFORE, in consideration of the mutual promises contained herein, MIPS and Broadcom agree to amend the 2007 License Agreement as provided below:

1. Section 12 of the 2007 License Agreement shall be deleted in its entirety and replaced by the following:

"12. LIMITATION OF LIABILITY

EXCEPT FOR BREACHES OF SECTION 2 ("LICENSE GRANTS') AND SECTION 9 ("CONFIDENTIAL INFORMATION), NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INCIDENTAL, INDIRECT, CONSEQUENTIAL, SPECIAL, OR PUNITIVE DAMAGES OF ANY KIND OR NATURE ARISING OUT OF THIS AGREEMENT, WHETHER SUCH LIABILITY IS ASSERTED ON THE BASIS OF CONTRACT, TORT (INCLUDING NEGLIGENCE OR STRICT LIABILITY), OR OTHERWISE, EVEN IF THE PARTY HAS BEEN WARNED OF THE POSSIBILITY OF ANY SUCH LOSS OR DAMAGE IN ADVANCE.

EXCEPT FOR AMOUNTS DUE UNDER SECTION 5, OR FOR BREACHES OF SECTIONS 2 AND/OR 9, IN NO EVENT SHALL BROADCOM'S OR MIPS' TOTAL LIABILITY UNDER THIS AGREEMENT (BUT EXCLUDING MIPS LIABILITY UNDER SECTION 11.1 ("INDEMNIFICATION BY MIPS') AND BROADCOM'S LIABILITY UNDER SECTION 11.2 ("INDEMNIFICATION BY BROADCOM) WHICH ARE COVERED BELOW), EXCEED $13,500,000.

NOTWITHSTANDING THE ABOVE, THE PARTIES AGREE THAT EXCEPT FOR AMOUNTS DUE UNDER THE LICENSE FEES AND ROYALTIES PROVISION, OR FOR BREACHES OF THE LICENSE GRANTS AND/OR CONFIDENTIAL INFORMATION PROVISION OF THIS AGREEMENT (BUT EXCLUDING MIPS LIABILITY UNDER SECTION 11.1 ("INDEMNIFICATION BY MIPS') AND BROADCOM'S LIABILITY UNDER SECTION 11.2 ("INDEMNIFICATION BY

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

BROADCOM) WHICH ARE COVERED BELOW), THE ORIGINAL AGREEMENT AND ANY SEPARATE AGREEMENT FOR MIPS ARCHITECTURE(S) OR MIPS CORE(S), THE TOTAL LIABILITY OF EITHER PARTY UNDER THIS AGREEMENT, THE ORIGINAL AGREEMENT AND ANY SEPARATE AGREEMENT FOR MIPS ARCHITECTURE(S) OR MIPS CORE(S) SHALL NOT EXCEED $13,500,000.

THE PARTIES AGREE THAT (1) MIPS' AGGREGATE LIABILITY FOR PATENT INFRINGEMENT INDEMNIFICATION UNDER SECTION 11.1 OF THIS AGREEMENT, SECTION 9.1 OF THE ORIGINAL AGREEMENT, SECTION 11.1 OF THAT CERTAIN MIPS16e ASE FOR MIPS32 ARCHITECTURE LICENSE AGREEMENT DATED FEBRUARY 10, 2004 ("2004 AGREEMENT") OR ANY INDEMNIFICATION LIABILITY FOR PATENT INFRINGEMENT INCURRED BY MIPS UNDER ANY SEPARATE AGREEMENT FOR MIPS ARCHITECTURE(S) OR MIPS CORE(S), AND (2) BROADCOM'S AGGREGATE LIABILITY FOR PATENT INFRINGEMENT INDEMNIFICATION UNDER SECTION 11.2 OF THIS AGREEMENT, SECTION 9.3 OF THE ORIGINAL AGREEMENT, SECTION 11.2 OF THE 2004 AGREEMENT OR ANY INDEMNIFICATION LIABILITY FOR PATENT INFRINGEMENT INCURRED BY BROADCOM UNDER ANY SEPARATE AGREEMENT FOR MIPS ARCHITECTURE(S) OR MIPS CORE(S), SHALL, IN THE CASE OF EACH PARTY, NOT EXCEED $5,000,000. IN THE EVENT EITHER PARTY'S INDEMNITY OBLIGATION UNDER SECTION 11 IS TRIGGERED, THE INDEMNIFYING PARTY AGREES TO WORK IN GOOD FAITH WITH THE INDEMNIFIED PARTY TO AVOID ANY DAMAGES TO THE INDEMNIFIED PARTY.

NOTWITHSTANDING ANYTHING TO THE CONTRARY IN THIS AGREEMENT, IN NO EVENT SHALL MIPS BE LIABLE FOR ANY DAMAGES RELATING TO OR RESULTING FROM THE USE OF MIPS TECHNOLOGY IN PRODUCTS USED FOR AVIATION, MEDICAL, NUCLEAR OR ULTRA HAZARDOUS PURPOSES OR FOR ANY DAMAGES OWED TO THIRD PARTIES RELATING TO TECHNOLOGY NOT PROVIDED BY MIPS. LIABILITY FOR DAMAGES SHALL BE LIMITED AND EXCLUDED AS SET FORTH HEREIN, EVEN IF ANY EXCLUSIVE REMEDY PROVIDED FOR IN THIS AGREEMENT FAILS OF ITS ESSENTIAL PURPOSE. EXCEPT AS OTHERWISE PROVIDED ABOVE, NOTHING IN THIS PROVISION LIMITS MIPS LIMITATION OF LIABILITY OBLIGATIONS WITH RESPECT TO MIPS DELIVERABLES LICENSED TO BROADCOM UNDER ANY OTHER AGREEMENT. EXCEPT AS OTHERWISE PROVIDED ABOVE, NOTHING IN THIS PROVISION LIMITS BROADCOM'S LIMITATION OF LIABILITY OBLIGATIONS WITH RESPECT TO MIPS UNDER ANY OTHER AGREEMENT."

2. The definition of the "Termination Date" in Section 13.1 of the 2007 License Agreement is hereby amended to be "December 31, 2028."

3. Section 2 of Exhibit D to the 2007 License Agreement shall be supplemented to add the following additional royalty provisions:

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

Licensed MIPS Core	**Royalty Per Unit of Broadcom Product in Year when Shipped**
	[*]
[*]	[*]

In the event a Broadcom Product includes [*] Licensed MIPS Core, Broadcom shall be obligated to pay a royalty [*] and [*]."

4. Maintenance fees under the 2007 License Agreement, as amended, and any applicable Technology Schedule, [*]. Thereafter, Broadcom may elect at its discretion upon written notice to MIPS to purchase maintenance under the 2007 License Agreement, as amended, and any applicable Technology Schedule for an annual maintenance fee of [*] for [*].

5. Section 14.5 is hereby amended to add the following sentences to the end of Section 14.5:

"In the event that Broadcom acquires a third party that has separately licensed architecture, cores or other technology from MIPS for which Broadcom also has a sufficient license, Broadcom may upon written notice to MIPS: (1) terminate such acquired third party's license with MIPS effective as of the closing date of the acquisition or such later date as Broadcom may reasonably specify in the notice, (2) if such third party is merged with and into Broadcom or otherwise ceases to be an operating company, Broadcom shall assume responsibility for all payments and other liabilities of such third party arising prior to the termination of the MIPS license; provided, however, that the terms and conditions of any patent license, covenant not to assert patents or similar provisions shall be limited to and shall solely relate to the patents issued or filed by such acquired third party prior to the effective date of the termination of the MIPS license, and (3) effective upon the termination of such third party's license with MIPS, such acquired third party and its products shall be subject to and governed by this Agreement or the applicable license agreement between Broadcom and MIPS, including with respect to all licenses, obligations, agreements, covenants, royalties and liabilities. The parties acknowledge that additional terms may be necessary in regards to specific Broadcom acquisitions, and upon request by Broadcom, the parties will negotiate such additional terms in good faith consistent with the terms set forth in the preceding sentence."

6. Except as expressly provided in this Amendment 6, all terms and conditions of the 2007 License Agreement shall remain unchanged and in full force and effect to the same extent as in full force and effect on the Amendment 6 Effective Date.

[Signature Page Follows]

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

IN WITNESS WHEREOF, the parties hereto have caused this Amendment 6 to be signed below by their respective duly authorized officers.

MIPS TECHNOLOGIES, INC.	**BROADCOM CORPORATION**
By: /s/ SANDEEP VIJ	By: /s/ DANIEL MAROTTA
Name: Sandeep Vij	Name: Daniel Marotta
Title: CEO	Title: SVP & GM Broadcom

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

Attachment 2
AMENDMENT 3 TO
LICENSE AGREEMENT

This Amendment 3 to License Agreement ("Amendment") is made effective as of June 29, 2012 (the "Amendment Effective Date") by and between Broadcom Corporation, a Delaware corporation with its principal place of business at 5300 California Avenue, Irvine, California 92617 ("Broadcom") and MIPS Technologies, Inc., a Delaware corporation with its principal place of business at 955 East Arques Ave., Sunnyvale, California 94085 ("MIPS"). Unless otherwise indicated below, any capitalized terms in this Amendment not defined herein shall have the applicable meaning set forth in the License Agreement between MIPS and Broadcom dated August 1998, as amended (the "1998 License Agreement").

WHEREAS, the parties desire to amend and extend certain terms of the 1998 License Agreement, as set forth herein;

NOW, THEREFORE, in consideration of the mutual promises contained herein, MIPS and Broadcom agree to amend the 1998 License Agreement as provided below:

1. Section 11.11 of the 1998 License Agreement shall be amended to add the following sentence to the end of such Section:

"THE PARTIES AGREE THAT THE PARTIES' AGGREGATE LIABILITY FOR PATENT INFRINGEMENT INDEMNIFICATION UNDER SECTION 9 OF THIS AGREEMENT SHALL BE SUBJECT TO THE AGGREGATE LIMITATION ON LIABILITY FOR PATENT INFRINGEMENT INDEMNIFICATION SET FORTH IN SECTION 12 OF THAT CERTAIN 2007 MIPS CORES LICENSE AGREEMENT BETWEEN MIPS AND BROADCOM DATED JANUARY 26, 2007, AS AMENDED."

2. The definition of the "Termination Date" in Section 10.1 of the 1998 License Agreement is hereby amended to be "December 31, 2028."

3. The 1998 License Agreement shall be supplemented to add the following additional royalty provisions covering the applicable years below:

Licensed MIPS Core	**Royalty Per Unit of Broadcom Product in Year when Shipped**
	[*]
[*]	[*]

In the event a Broadcom Product includes [*] Licensed MIPS Core, Broadcom shall be obligated to pay a royalty [*] and [*]."

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

4. Maintenance fees under the 1998 License Agreement, as amended, and any applicable Technology Schedule, [*].

5. Section 11.6 is hereby amended to add the following sentences to the end of Section 11.6:

"In the event that Broadcom acquires a third party that has separately licensed architecture, cores or other technology from MIPS for which Broadcom also has a sufficient license, Broadcom may upon written notice to MIPS: (1) terminate such acquired third party's license with MIPS effective as of the closing date of the acquisition or such later date as Broadcom may reasonably specify in the notice, (2) if such third party is merged with and into Broadcom or otherwise ceases to be an operating company, Broadcom shall assume responsibility for all payments and other liabilities of such third party arising prior to the termination of the MIPS license; provided, however, that the terms and conditions of any patent license, covenant not to assert patents or similar provisions shall be limited to and shall solely relate to the patents issued or filed by such acquired third party prior to the effective date of the termination of the MIPS license, and (3) effective upon the termination of such third party's license with MIPS, such acquired third party and its products shall be subject to and governed by this Agreement or the applicable license agreement between Broadcom and MIPS, including with respect to all licenses, obligations, agreements, covenants, royalties and liabilities. The parties acknowledge that additional terms may be necessary in regards to specific Broadcom acquisitions, and upon request by Broadcom, the parties will negotiate such additional terms in good faith consistent with the terms set forth in the preceding sentence. ."

6. Except as expressly provided in this Amendment, all terms and conditions of the 1998 License Agreement shall remain unchanged and in full force and effect to the same extent as in full force and effect on the Amendment Effective Date.

[Signature Page Follows]

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

IN WITNESS WHEREOF, the parties hereto have caused this Amendment to be signed below by their respective duly authorized officers.

MIPS TECHNOLOGIES, INC.	**BROADCOM CORPORATION**
By: /s/ SANDEEP VIJ	By: /s/ DANIEL MAROTTA
Name: Sandeep Vij	Name: Daniel Marotta
Title: CEO	Title: SVP & GM Broadcom

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

Attachment 3
AMENDMENT TO
ARCHITECTURE LICENSE AGREEMENT

This Amendment to Architecture License Agreement ("Amendment") is made effective as of June 29, 2012 (the "Amendment Effective Date") by and between Broadcom Corporation, a Delaware corporation with its principal place of business at 5300 California Avenue, Irvine, California 92617 ("Broadcom") and MIPS Technologies, Inc., a Delaware corporation with its principal place of business at 955 East Arques Ave., Sunnyvale, California 94085 ("MIPS"). Unless otherwise indicated below, any capitalized terms in this Amendment not defined herein shall have the applicable meaning set forth in the MIPS16e ASE for MIPS32 Architecture License Agreement dated February 10, 2004, as amended, between MIPS and Broadcom, as amended (the "2004 License Agreement").

WHEREAS, the parties desire to amend and extend certain terms of the 2004 License Agreement, as set forth herein;

NOW, THEREFORE, in consideration of the mutual promises contained herein, MIPS and Broadcom agree to amend the 2004 License Agreement as provided below:

1. Section 12 of the 2004 License Agreement shall be amended to add the following sentence to the end of such Section:

"THE PARTIES AGREE THAT THE PARTIES' AGGREGATE LIABILITY FOR PATENT INFRINGEMENT INDEMNIFICATION UNDER SECTION 11 OF THIS AGREEMENT SHALL BE SUBJECT TO THE AGGREGATE LIMITATION ON LIABILITY FOR PATENT INFRINGEMENT INDEMNIFICATION SET FORTH IN SECTION 12 OF THAT CERTAIN 2007 MIPS CORES LICENSE AGREEMENT BETWEEN MIPS AND BROADCOM DATED JANUARY 26, 2007, AS AMENDED."

2. The definition of the "Termination Date" in Section 13.1 of the 2004 License Agreement is hereby amended to be "December 31, 2028."

3. The 2004 License Agreement shall be supplemented to add the following additional royalty provisions covering the applicable years below:

Licensed MIPS Core	**Royalty Per Unit of Broadcom Product in Year when Shipped**
	[*]
[*]	[*]

In the event a Broadcom Product includes [*] Licensed MIPS Core, Broadcom shall be obligated to pay a royalty [*] and [*]."

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

4. Maintenance fees under the 2004 License Agreement, as amended, and any applicable Technology Schedule, [*].

5. Section 14.5 is hereby amended to add the following sentences to the end of Section 14.5:

"In the event that Broadcom acquires a third party that has separately licensed architecture, cores or other technology from MIPS for which Broadcom also has a sufficient license, Broadcom may upon written notice to MIPS: (1) terminate such acquired third party's license with MIPS effective as of the closing date of the acquisition or such later date as Broadcom may reasonably specify in the notice, (2) if such third party is merged with and into Broadcom or otherwise ceases to be an operating company, Broadcom shall assume responsibility for all payments and other liabilities of such third party arising prior to the termination of the MIPS license; provided, however, that the terms and conditions of any patent license, covenant not to assert patents or similar provisions shall be limited to and shall solely relate to the patents issued or filed by such acquired third party prior to the effective date of the termination of the MIPS license, and (3) effective upon the termination of such third party's license with MIPS, such acquired third party and its products shall be subject to and governed by this Agreement or the applicable license agreement between Broadcom and MIPS, including with respect to all licenses, obligations, agreements, covenants, royalties and liabilities. The parties acknowledge that additional terms may be necessary in regards to specific Broadcom acquisitions, and upon request by Broadcom, the parties will negotiate such additional terms in good faith consistent with the terms set forth in the preceding sentence."

6. Except as expressly provided in this Amendment, all terms and conditions of the 2004 License Agreement shall remain unchanged and in full force and effect to the same extent as in full force and effect on the Amendment Effective Date.

[Signature Page Follows]

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

IN WITNESS WHEREOF, the parties hereto have caused this Amendment to be signed below by their respective duly authorized officers.

MIPS TECHNOLOGIES, INC.	**BROADCOM CORPORATION**
By: /s/ SANDEEP VIJ	By: /s/ DANIEL MAROTTA
Name:Sandeep Vij	Name:Daniel Marotta
Title: CEO	Title: SVP & GM Broadcom

[*] Certain portions denoted with an asterisk have been omitted and filed separately with the Securities and Exchange Commission. Confidential treatment has been requested with respect to the omitted portions.

Exhibit 31.5

FORM 10-K CERTIFICATION

I, Sandeep Vij, certify that:

1. I have reviewed this amendment no. 2 to the annual report on Form 10-K of MIPS Technologies, Inc.;

2. Based on my knowledge, this report does not contain any untrue statement of a material fact or omit to state a material fact necessary to make the statements made, in light of the circumstances under which such statements were made, not misleading with respect to the period covered by this report;

Date: January 11, 2013

By: /s/ SANDEEP VIJ
Sandeep Vij
President and Chief Executive Officer,
MIPS Technologies, Inc.

Exhibit 31.6

FORM 10-K CERTIFICATION

I, William Slater, certify that:

1. I have reviewed this amendment no. 2 to the annual report on Form 10-K of MIPS Technologies, Inc.;

2. Based on my knowledge, this report does not contain any untrue statement of a material fact or omit to state a material fact necessary to make the statements made, in light of the circumstances under which such statements were made, not misleading with respect to the period covered by this report;

Date: January 11, 2013

By: /s/ WILLIAM SLATER
William Slater
Vice President and Chief Financial Officer,
MIPS Technologies, Inc.